



Package Type : PP-1S

Product Features

- TD-LTE band 3400~3600MHz
- Power gain 25dB, Psat 50W
- Main Doherty amp. efficiency 45% @ Pavg=9W
- Input/Output Impedance 50ohm
- 2-Stage Doherty Amplifier
- GaN on SiC Technology
- Copper clad laminates board
- 13x17x2.2mm size SMD package

Applications

- Massive MIMO
- 4G/5G LTE Technology
- TDD or FDD- LTE system
- AAS(Active Antenna System)
- Small cell

Description

The RPAM35008-25 is a fully integrated micro-strip Doherty GaN Hybrid power amplifier module designed for applications in 5G Massive MIMO systems, small cells, and low power remote radio heads. RPAM Series is an integrated 2-stage power amplifier module, 50ohm input and output impedance matched device can deliver up to 50W of saturation power. This device is size 13x17x2.2mm and is packaged in a plastic surface mount package.

Electrical Specifications @ Vds=28V, Ta=25°C

PARAMETER	UNIT	MIN	TYP	MAX	CONDITION
Frequency Range	MHz	3400	3500	3600	ZS = ZL = 50 ohm
Power Gain		-	25	-	
Gain Flatness	dB	-1.5	-	+1.5	-
Input Return Loss		-	-12	-	
Pout @ Average	dBm	-	39	-	8W
Pout @ Saturation	dBm	-	47	-	Pulse Width=20us, Duty cycle 10%
ACLR @ BW 20MHz 1FA LTE (PAPR 7.0dB)	dBc	-	-28	-25	Non DPD
		-	-54	-	With DPD
Doherty Efficiency	%	-	45	-	Pavg=9W
Total Efficiency		-	41	-	
Supply Voltage	V	-4.9	-2.8	-2.0	Vgd
		-4.9	-2.8	-2.0	Vgc
		-4.9	-4.8	-3.0	Vgp
		-	28	-	Vds

Caution

The drain voltage must be supplied to the device after the gate voltage is supplied

Turn on → Turn on the Gate voltage supply and last turn on the Drain voltage supplies

Turn off → Turn off the Drain voltage and last turn off the Gate voltage

Note

1. ACLR Measured Pout=39dBm @ fc± 20MHz / 18.03MHz

LTE 20MHz 1FA PAPR=7.0dB @ 0.01% probability on CCDF

Mechanical Specifications

PARAMETER	UNIT	TYPICAL	RATING
Mass	g	4.0	-
Dimension	mm	13 x 17 x 2.2	±0.15

Absolute Maximum Ratings

PARAMETER	UNIT	RATING	SYMBOL	CONDITION
Gate-Source Voltage	V	-10 ~ 0	V _{gd} V _{gc} V _{gp}	T _c =25°C
Drain-Source Voltage	V	50	V _{ds}	T _c =25°C
Gate Current	mA	1.2 3.6 7.2	Drive Carrier Peaking	T _c =25°C
Power Dissipation	W	23	P _D	T _c =85°C
Operating Junction Temperature	°C	225	T _J	-
Operating Case Temperature	°C	-30 ~ 85	T _C	-
Storage Temperature	°C	-40 ~ 100	T _{STG}	-
Soldering Temperature ^{*1}	°C	260	T _s	30s Max.
RF Input Level (Pulse)	dBm	34	Pin	T _c =25°C

*1 Reflow cycle limit : 1time

Operating Voltages & Input level

PARAMETER	UNIT	MIN	TYP	MAX	SYMBOL
Drain Voltage 1	V	27.5	28	28.5	V _{ds1}
Drain Voltage 2	-	27.5	28	28.5	V _{ds2}
Gate Voltage (on-state)	V	-4.9	V _{gd} ^{*2}	-2.0	V _{gd}
Gate Voltage (on-state)	V	-4.9	V _{gc} ^{*3}	-2.0	V _{gc}
Gate Voltage (on-state)	V	-4.9	V _{gp} ^{*4}	-3.0	V _{gp}
Gate Voltage (off-state)	V	-	-8	-	V _{gd}
Gate Voltage (off-state)	V	-	-8	-	V _{gc}
Gate Voltage (off-state)	V	-	-8	-	V _{gp}
RF Input Level (Pulse)	dBm	-	-	30	Pin

*2 V_{gd}(Pin#28) set : Drive amp. Idq 30mA

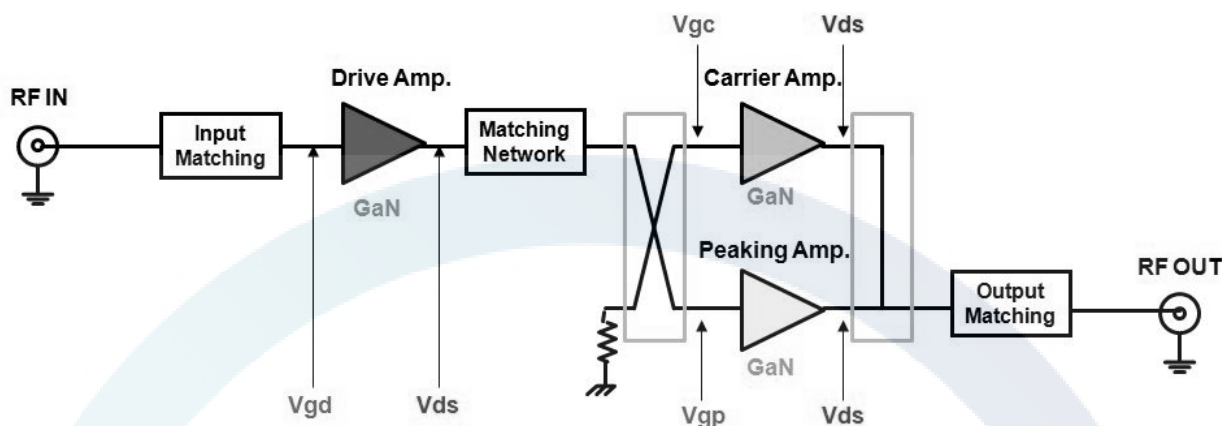
*3 V_{gc}(Pin#25) set: Carrier Idq 100mA±5%

*4 V_{gp}(Pin#8) set: Lower V_{gp} of Δ-1.9V at Peaking Idq 10mA

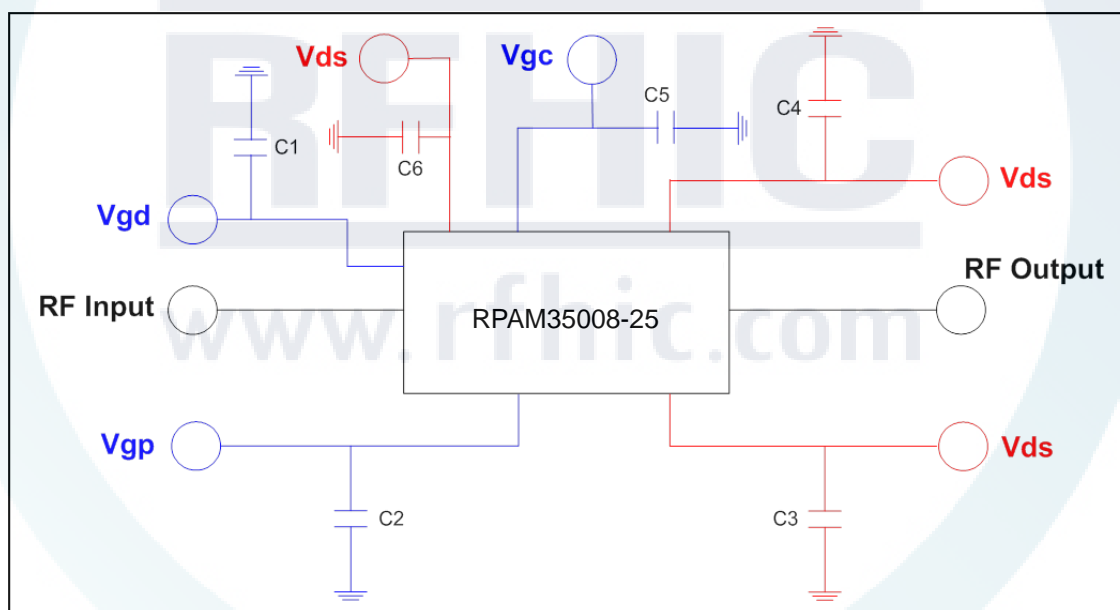
ESD Level

PARAMETER	STANDARD	RESULT
HBM	JESD22-A114E	Class 1A/ passed Voltage 500V
MM	JESD22-A115C	Class A/ passed Voltage 100V

Block Diagram



Application Circuit



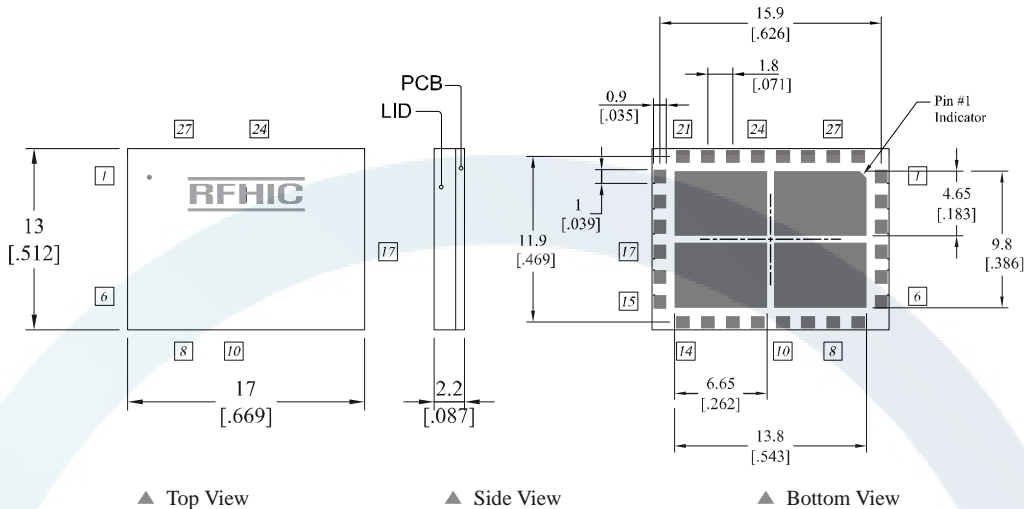
Bill of Material (Evaluation board)

LOCATION	Part Number	Value	Manufacturer
C3, C4, C6	1812B225K101CT	2.2uF / 100V	WALSIN
C1, C2, C5	GRM1885C1H101JA01D	100pF / 50V	MURATA
PCB	RO4350B	2Layer, 20mil, 1oz	ROGERS

Package Dimensions (Type: PP-1R)

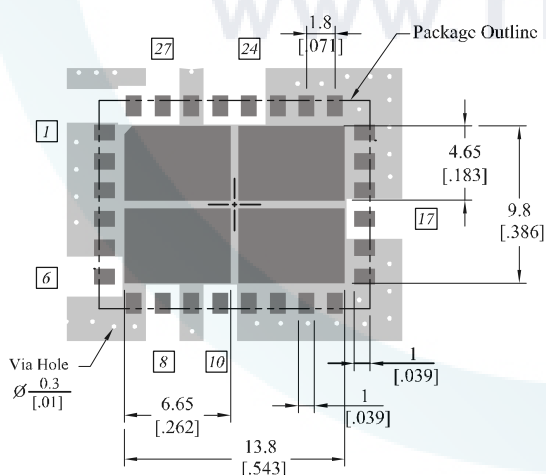
* Unit: mm[inch] | Tolerance: ±0.15[.006]

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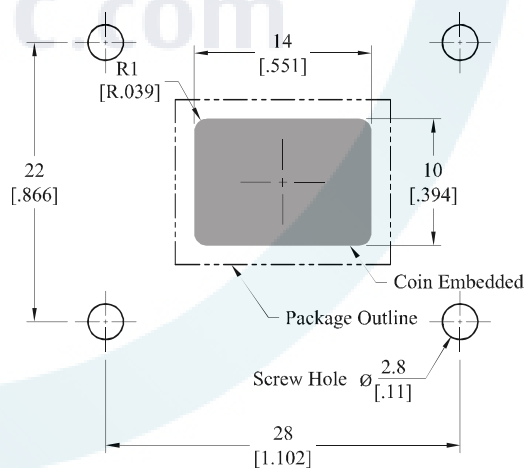


Pin Description							
Pin No	Function	Pin No	Function	Pin No	Function	Pin No	Function
6	RF In	10	Vds	24	Vds	27	Vds
8	Vgp	17	RF Out	25	Vgc	28	Vgd
All other pins Ground							

Recommended Pattern



Mounting Configuration & Coin Embedded



*** Mounting Configuration Notes**

1. For the proper performance of the device, Ground / Thermal via holes must be designed to remove heat.
2. To properly use heatsink, ensure the ground/thermal via hole region to contact the heatsink. We recommend the mounting screws be added near the heatsink to mount the board
3. In designing the necessary RF trace, width will depend upon the PCB material and construction.
4. Use 1 oz. Copper minimum thickness for the heatsink.
5. Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink
6. We recommend adding as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
7. We recommend that the PCB with the RF device in a hybrid package is not washed to remove the flux.

Ordering Information

Part Number	Package Design
RPAM35008-25	-R (Reel)
	-B (Bulk)
	-EVB (Evaluation Board)

Revision History

Part Number	Release Date	Version	Modification	Data Sheet Status
RPAM35008-25	2018.12.21	0.1	Initial release	Preliminary



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