

# TRA\_120\_002

120-GHz Highly Integrated IQ Transceiver with Antennas on Chip  
in Silicon Germanium Technology

## Preliminary Data Sheet

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## Version Control

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Version	Changed section	Description of change	Reason for change
0.5	template	Sections version control and document release added	controlled document
0.6	specification	Spec data revised	routinely revision
0.7	6.5 VCO Tuning Inputs	Information parameter and application hint added	update
	6.2 Power Cycling	Application hint added	update
	7 Meas. Results	Antenna Radiation Pattern (Fig. 17, 18) added	update
0.8	5.4 Qualification Test	Section with reflow profile added	update

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# 1 Features

- Radar front end (RFE) with on-chip antennas for 122-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 380 mW in continuous operating mode
- Integrated low phase noise push-push VCO
- Receiver with homodyne quadrature mixer
- RX and TX dipole on-chip antennas
- Large bandwidth of up to 7 GHz
- QFN32 leadless plastic package 5 × 5 mm<sup>2</sup>
- Pb-free, RoHS compliant package
- IC is available as bare die as well



## 1.1 Overview

The radar front end TRA\_120\_002 is an integrated transceiver circuit for the 122-GHz ISM band with antennas on chip. It includes a low-noise amplifier (LNA), quadrature mixers, a poly-phase filter, a voltage controlled oscillator, divide-by-32 outputs, and transmit and receive antennas (see Figure 1).

The RF signal from the oscillator is directed to the RX path via buffer circuits. The RX signal is amplified by the LNA and converted to baseband by two mixers with quadrature local oscillator (LO). The 120-GHz LO has four analog tuning inputs with different tuning ranges and tuning slopes. The tuning inputs can be combined to obtain a wide frequency tuning range. The analog tuning inputs together with the integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing analog tuning inputs.

The IC is fabricated in SG13S SiGe BiCMOS technology of IHP GmbH.

## 1.2 Applications

The main field of application for the 120-GHz transceiver radar frontend (RFE) is in short range radar systems with a range up to about 10 meters. By using dielectric lenses, the range can be increased considerably. The RFE can be used in FMCW mode as well as in CW mode. Although the chip is intended for use in the ISM band 122 GHz - 123 GHz, it is also possible to extend the bandwidth to the full tuning range of 7 GHz.

## 2 Block Diagram

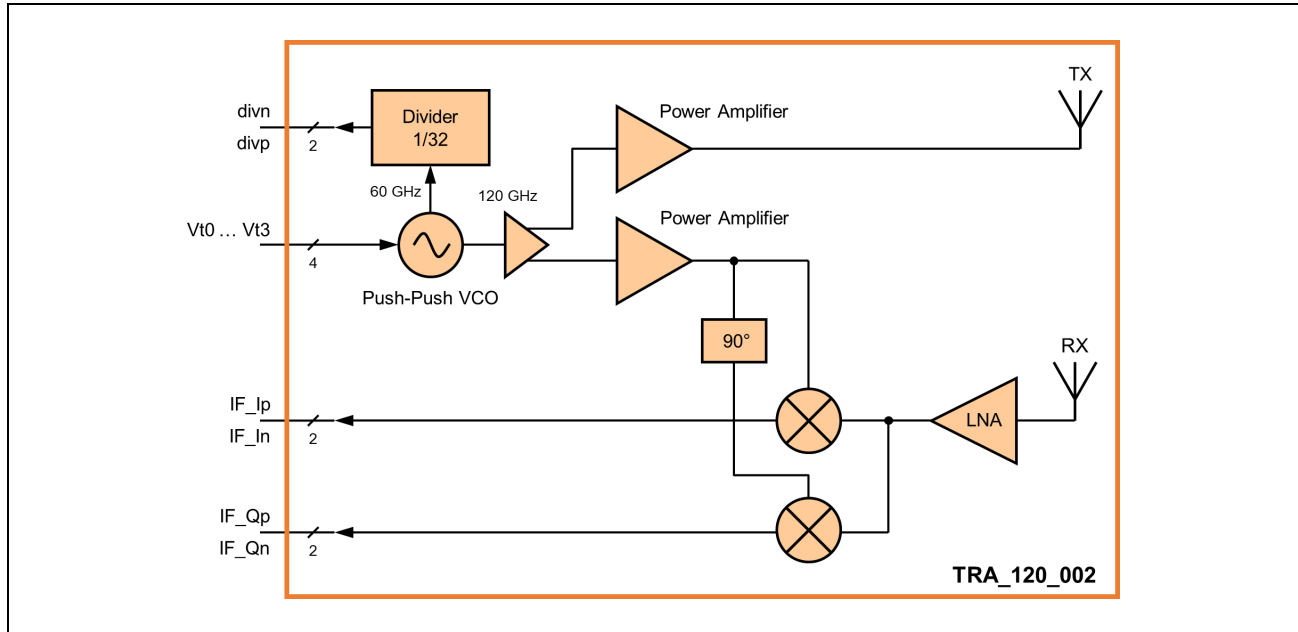


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment

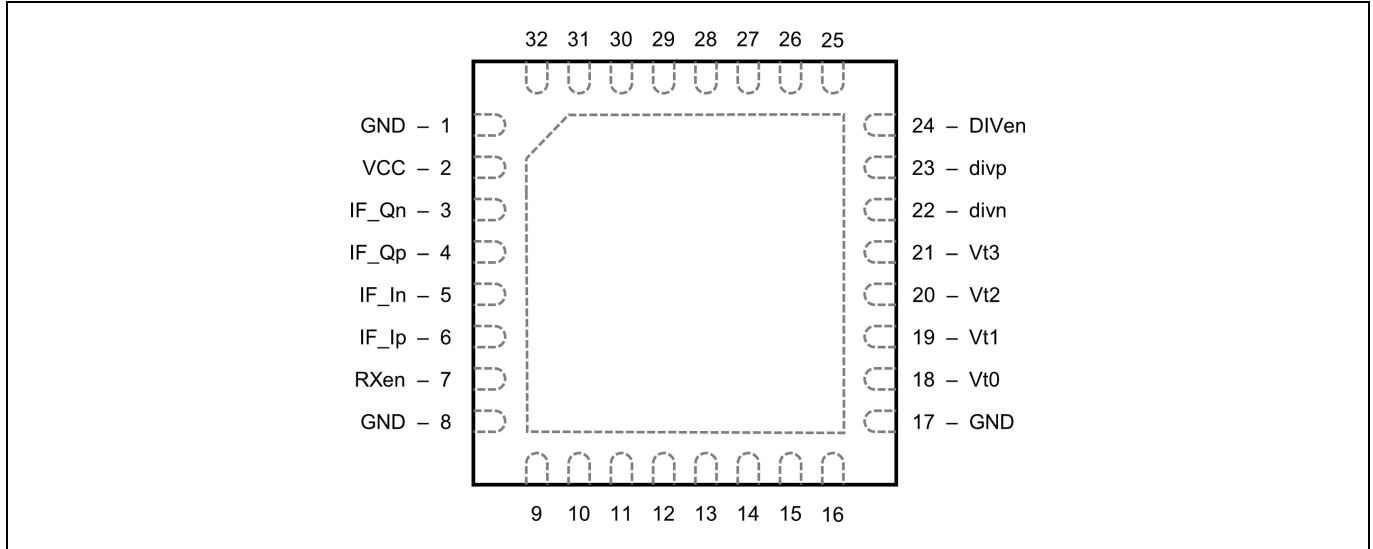


Figure 2 Pin Assignment (QFN32, top view)

#### 3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
2	VCC	Supply voltage (3.3 V)
3	IF_Qn	Quadrature IF I output, negative terminal (DC coupled)
4	IF_Qp	Quadrature IF I output, positive terminal (DC coupled)
5	IF_In	Quadrature IF Q output, negative terminal (DC coupled)
6	IF_Ip	Quadrature IF Q output, positive terminal (DC coupled)
7	RXen	Receiver enable input, low-active CMOS input with internal 70-kΩ pull-down resistor
18	Vt0	VCO tuning input 0 (0 – V <sub>CC</sub> )
19	Vt1	VCO tuning input 1 (0 – V <sub>CC</sub> )
20	Vt2	VCO tuning input 2 (0 – V <sub>CC</sub> )
21	Vt3	VCO tuning input 3 (0 – V <sub>CC</sub> )
22	divn	Divider output, neg. terminal. 50 Ω, DC coupled, external decoupling cap. required
23	divp	Divider output, pos. terminal. 50 Ω, DC coupled, external decoupling cap. required
24	DIVen	Divider enable input, low-active CMOS input with internal 100-kΩ pull-down resistor
9 - 16, 25 - 32	NC	Not connected. These pins may be connected to ground. Performance will not be affected.
1,8, 17	GND	Ground pins, also connected to the exposed die attach pad.
(33)	GND	Exposed die attach pad of the QFN package, must be soldered to ground.

## 4 Specification

### 4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply voltage	V <sub>CC</sub>		3.6	V	to GND
DC voltage at tuning inputs	V <sub>Vt</sub>	-0.3	V <sub>CC</sub> + 0.3	V	Inputs Vt0, Vt1, Vt2, Vt3
DC voltage at enable inputs	V <sub>EN</sub>	-0.3	V <sub>CC</sub> + 0.3	V	Inputs DIVen, RXen
Junction temperature	T <sub>J</sub>	-50	150	°C	
Storage temperature range	T <sub>STG</sub>	-65	150	°C	
ESD robustness	V <sub>ESD</sub>		1.2	kV	Human body model, HBM <sup>1)</sup>

1) CLASS 1C according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

### 4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Ambient temperature	T <sub>A</sub>	-40	85	°C	
Supply voltage	V <sub>CC</sub>	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning inputs	V <sub>Vt</sub>	0	V <sub>CC</sub>	V	Inputs Vt0 – Vt3
DC voltage at enable inputs	V <sub>EN</sub>	0	V <sub>CC</sub>	V	Inputs DIVen, RXen

**Note: Do not drive input signals without power supplied to the device.**

### 4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
Thermal resistance, junction-to-ambient	R <sub>thja</sub>	-	-	50	K/W	JEDEC standard JESD-51-5

#### 4.4 Electrical Characteristics

T<sub>A</sub> = -40 °C to +85 °C unless otherwise noted. Typical values measured at T<sub>A</sub> = 25 °C and V<sub>CC</sub> = 3.3 V.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
<b>DC Parameters</b>						
Supply current consumption	I <sub>CC</sub>		128	155	mA	RX and divider enabled
DIVen input voltage, low level	V <sub>DIVen_L</sub>	0		0.3 × V <sub>CC</sub>	V	Input DIVen
DIVen input voltage, high level	V <sub>DIVen_H</sub>	0.7 × V <sub>CC</sub>		V <sub>CC</sub>	V	Input DIVen
RXen input voltage, low level	V <sub>RXen_L</sub>	0		0.5 × V <sub>CC</sub>	V	Input RXen
RXen input voltage, high level	V <sub>RXen_H</sub>	V <sub>CC</sub> - 0.4		V <sub>CC</sub>	V	Input RXen
VCO tuning voltage	V <sub>VT</sub>	0		V <sub>CC</sub>	V	Inputs Vt0 – Vt3
<b>RF Parameters</b>						
VCO start frequency	f <sub>TX</sub>	117.8	119.3	120.8	GHz	Vt0 = Vt1 = Vt2 = Vt3 = 0
VCO stop frequency	f <sub>TX</sub>	124.3	125.8	127.3	GHz	Vt0 = Vt1 = Vt2 = Vt3 = 3.3 V
VCO tuning full bandwidth	Δf <sub>TX</sub>	5.5	6.5	7.5	GHz	Vt0 – Vt3 interconnected
Number adjustable of frequency bands		8				Vt1 – Vt3 used for band switching
Pushing VCO	Δf <sub>TX</sub> /ΔV <sub>CC</sub>		27		MHz/V	
Phase noise	P <sub>N</sub>		-90	-88	dBc/Hz	at 1 MHz offset
Transmitter output power	P <sub>TX</sub>	-7	-3	1	dBm	Measured without antennas
Divider ratio of TX signal	N <sub>DIV</sub>	64				
Divider output power	P <sub>DIV</sub>	-10		-7	dBm	Note 1
Divider output frequency	f <sub>DIV</sub>	1.85		1.98	GHz	
Receiver gain			8	10	dB	Measured without antennas
IF frequency range	f <sub>IF</sub>	0		200	MHz	
IF output impedance	Z <sub>OUT</sub>		500		Ω	Differential outputs
IQ amplitude imbalance			tbd		dB	
IQ phase imbalance		-10		10	deg	
Noise figure (DSB)			8.7		dB	Simulated, at f <sub>IF</sub> = 1 MHz)
Input compression point	1dB ICP		-20		dBm	Measured without antennas

Note 1 Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.



## 5 Packaging

### 5.1 Outline Dimensions

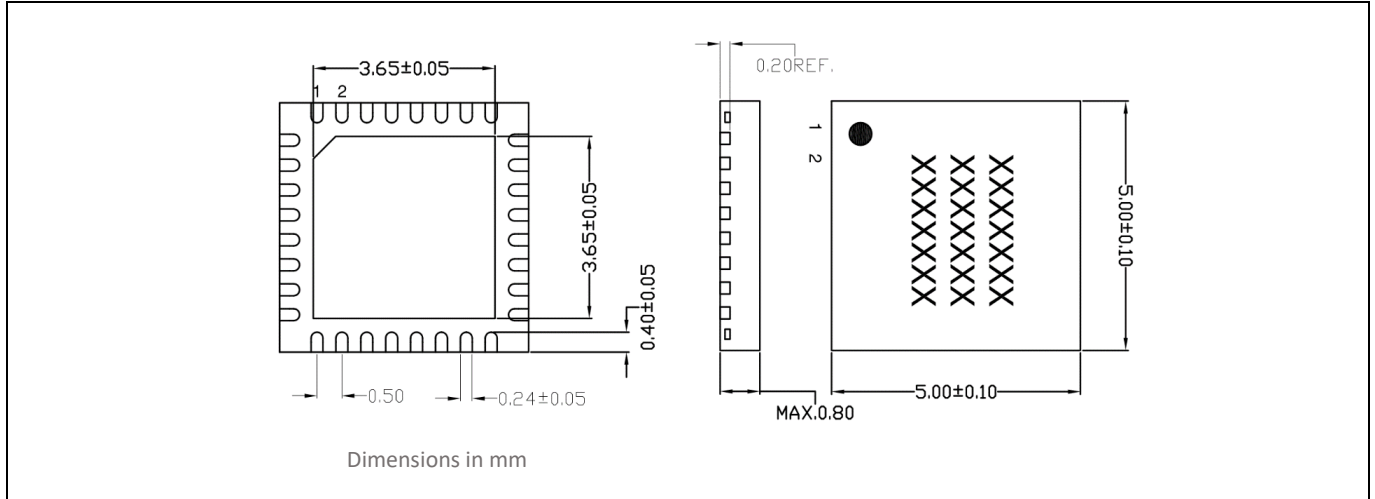


Figure 3 Outline Dimensions of QFN32 Package with Exposed Pad

### 5.2 Package Code

Top-Side Markings

TRA002  
 YYWW

### 5.3 Antenna Position

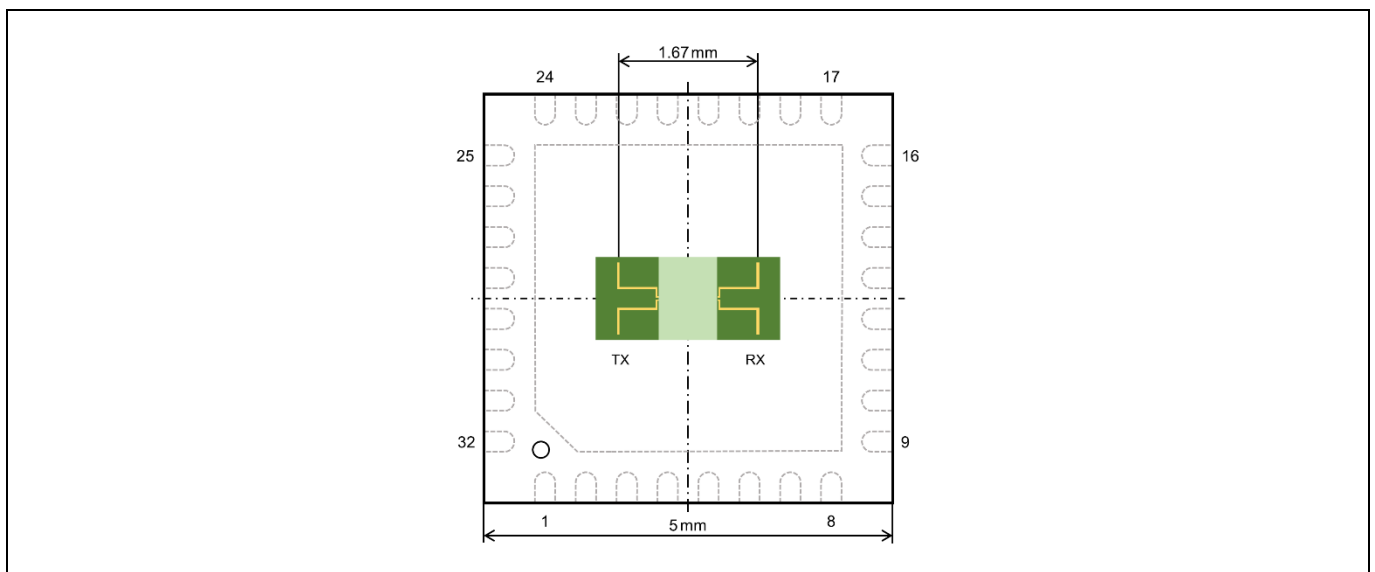


Figure 4 Antenna Position (top view)

## 5.4 Qualification Test

Table 6 Reliability and Environmental Test

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	pass

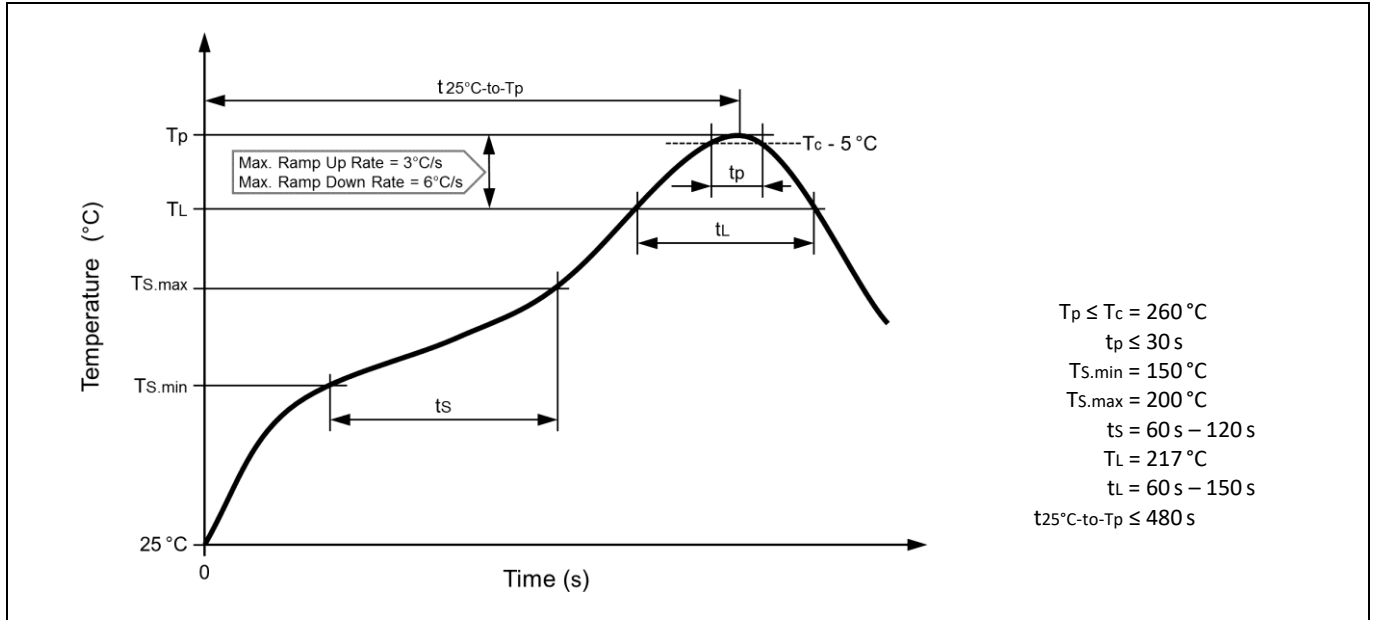


Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

## 6 Application

### 6.1 Application Circuit

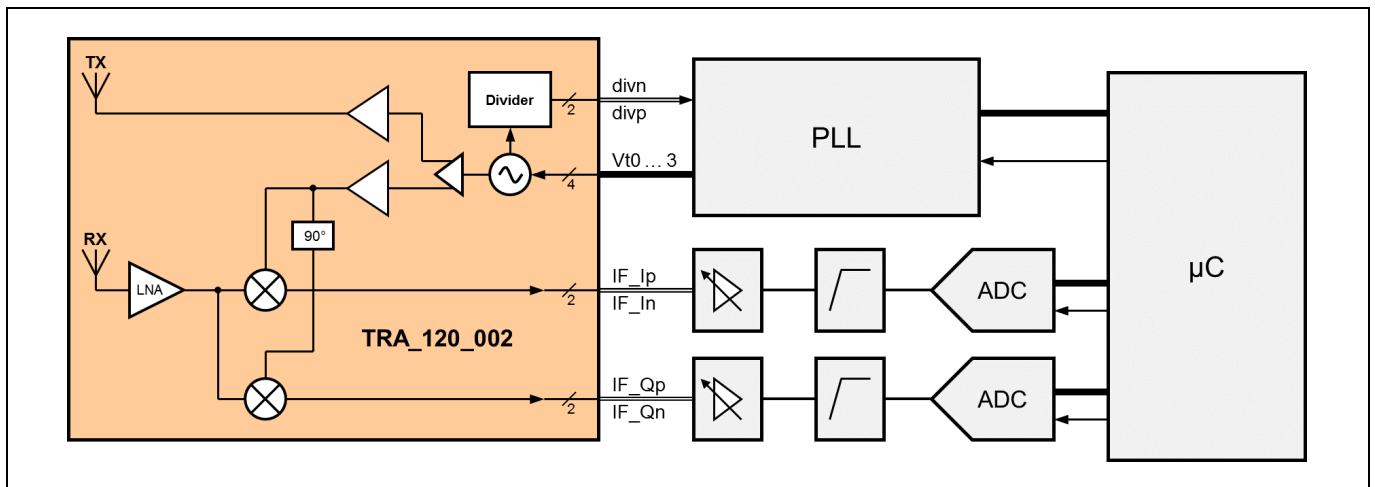


Figure 6 Application Circuit

## 6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100  $\mu$ s is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

## 6.3 Evaluation Boards

For a quick and easy start into radar development Silicon Radar offers SiRad Easy<sup>®</sup>. It is an evaluation board system for many of our integrated IQ transceivers with antennas in package or on PCB. It comes with a reference hardware and provides a complete design environment which can be configured via a browser-based graphical user interface. Its rich functionality and the open communication protocol make it a versatile tool – also for enhanced development projects.

It features:

- Distance measurement
- Velocity measurement
- Frequency modulated continuous wave mode (FMCW)
- Continuous wave mode (CW)

For more information about the features of SiRad Easy<sup>®</sup> see:

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## 6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds  $V_{CC}$  by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

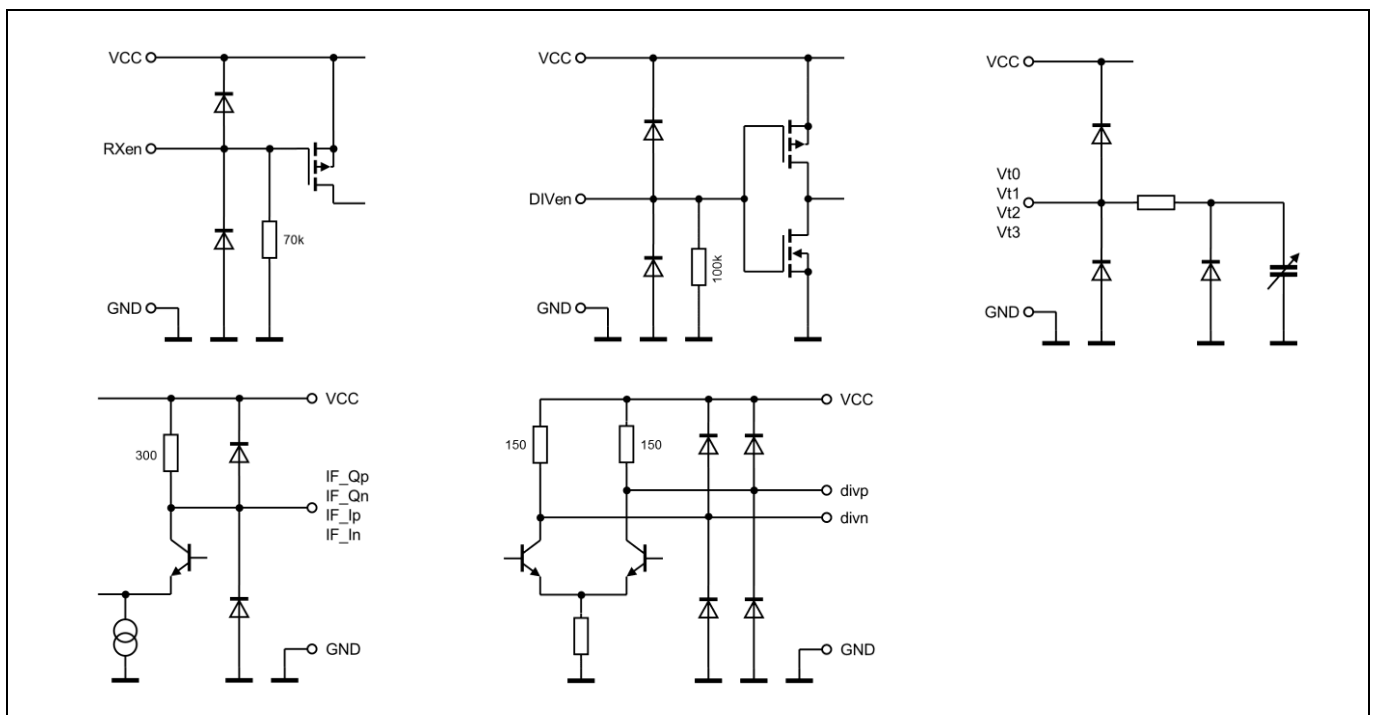


Figure 7 Equivalent I/O Circuits

## 6.5 VCO Tuning Inputs

The VCO tuning inputs Vt0 – Vt3 are of analog nature, but can be switched digitally as well. The tuning inputs differ in their tuning ranges (tuning bandwidth) and slopes, whereby Vt3 has the widest tuning range, and Vt0 the narrowest.

Table 7 Typical VCO Tuning Bandwidth and Slope

Input	VCO tuning bandwidth (MHz)		Middle band slope (MHz/V)	
Vt0	$\Delta f_{TX,Vt0}$	720	$\Delta f_{TX} / \Delta V_{Vt0}$	290
Vt1	$\Delta f_{TX,Vt1}$	750	$\Delta f_{TX} / \Delta V_{Vt1}$	300
Vt2	$\Delta f_{TX,Vt2}$	1580	$\Delta f_{TX} / \Delta V_{Vt2}$	630
Vt3	$\Delta f_{TX,Vt3}$	3450	$\Delta f_{TX} / \Delta V_{Vt3}$	1380

The VCO tuning range of a specific tuning input can be increased by connecting it to another tuning input. All combinations of the four tuning inputs are allowed. Unused tuning inputs must be set to a fixed potential (between 0 and V<sub>CC</sub>). The interconnection of all inputs Vt0 – Vt3 leads to the maximum tuning bandwidth. For example, if Vt0 is used as tuning input, the variation of the potential at Vt1, Vt2, Vt3 in all logical combinations of 0 and V<sub>CC</sub>, results in offsetting the tuning curve (see Figure 10).

## 6.6 Antenna Performance

The simulated gain of TX and RX on-chip antennas shows 10 dBi at an angle of 30°, see Figure 17 and 18.

## 7 Measurement Results

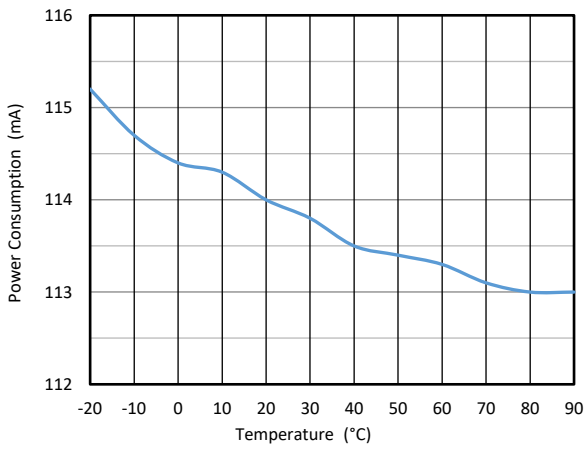


Figure 8 Power Consumption vs. Temperature

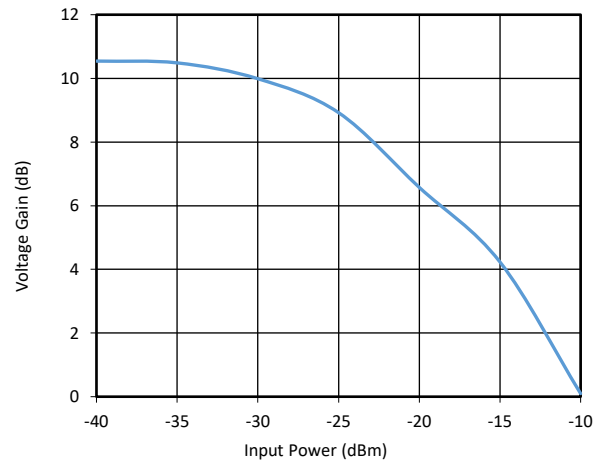


Figure 9 Conversion Gain of the Receiver (without antenna)

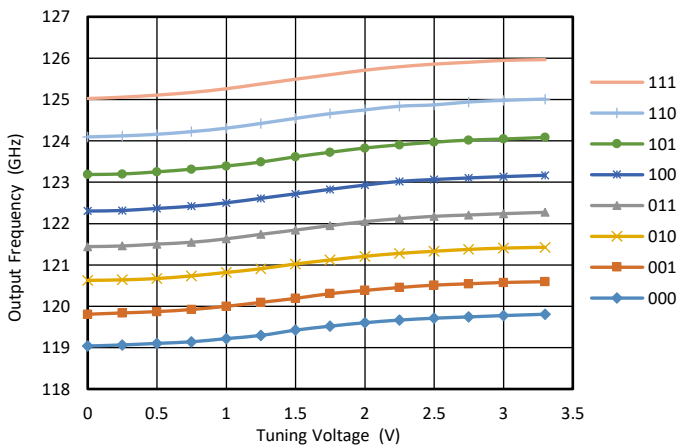


Figure 10 VCO Tuning Curves.  $V_{t0}$  is varied, while  $V_{t1}$ ,  $V_{t2}$  and  $V_{t3}$  are driven high or low. For example, 011 means  $V_{t3} = 0$ ,  $V_{t2} = 3.3\text{ V}$  and  $V_{t1} = 3.3\text{ V}$ .

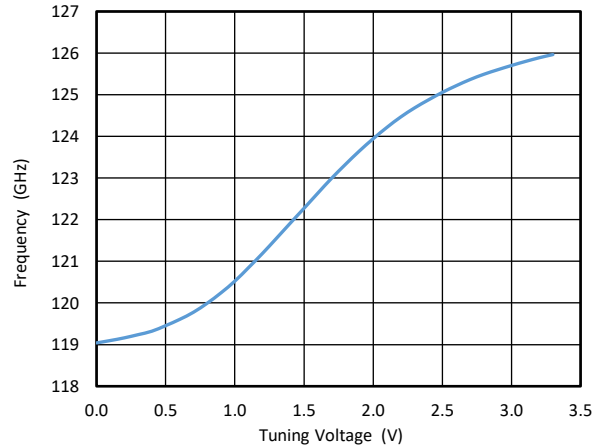


Figure 11 Full Bandwidth VCO Tuning.  $V_{t0}$ ,  $V_{t1}$ ,  $V_{t2}$ ,  $V_{t3}$  are interconnected. ( $V_{t0} = V_{t1} = V_{t2} = V_{t3}$ )

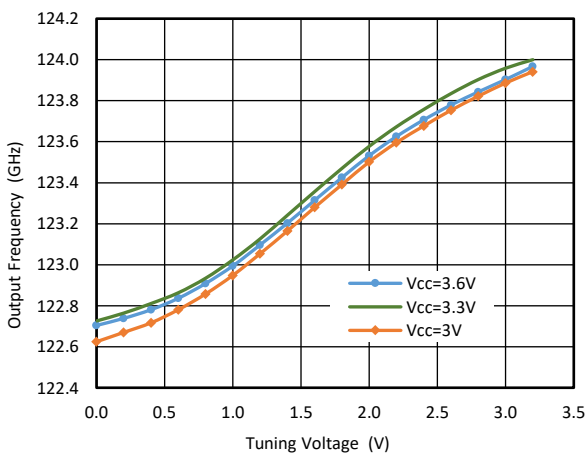


Figure 12 VCO Pushing -  $V_{cc} \pm 300\text{ mV}$   
 $V_{t0} = \text{Sweep}$ ,  $V_{t1} = V_{t2} = 0$ ,  $V_{t3} = 3.3\text{ V}$

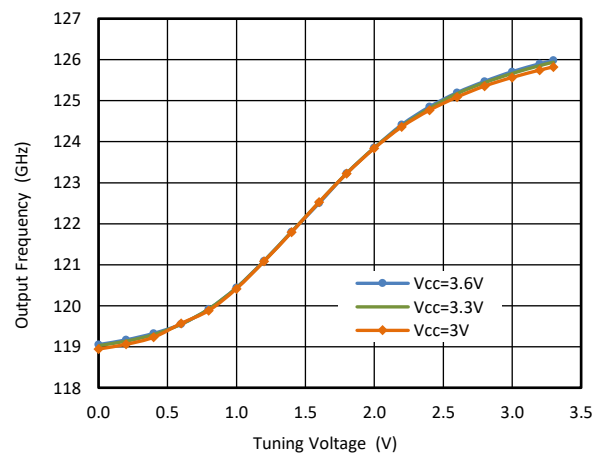


Figure 13 VCO Pushing - Full Bandwidth Operation. All tuning voltages,  $V_{t0} = V_{t1} = V_{t2} = V_{t3}$

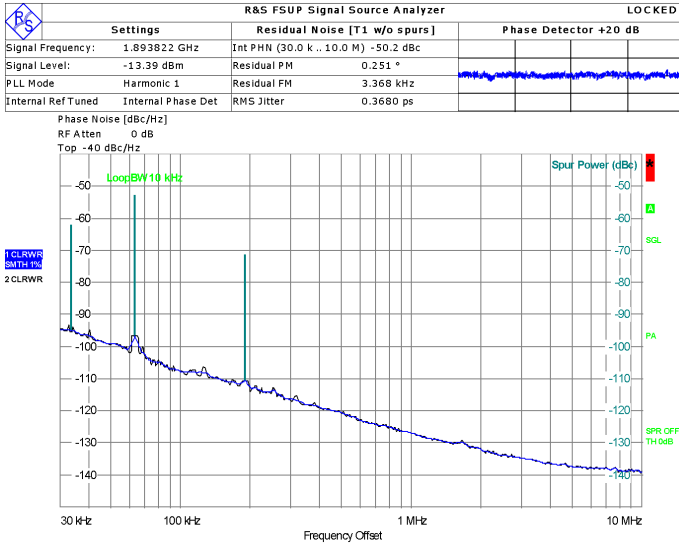


Figure 14 Phase Noise of the Integrated Oscillator at Divider Output (1.89 GHz)

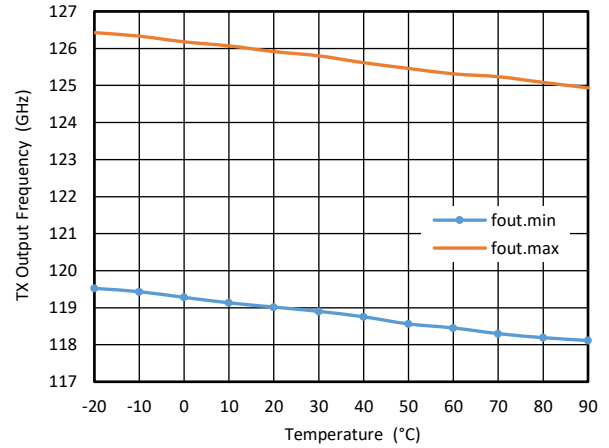


Figure 15 Output Frequency vs. Temperature

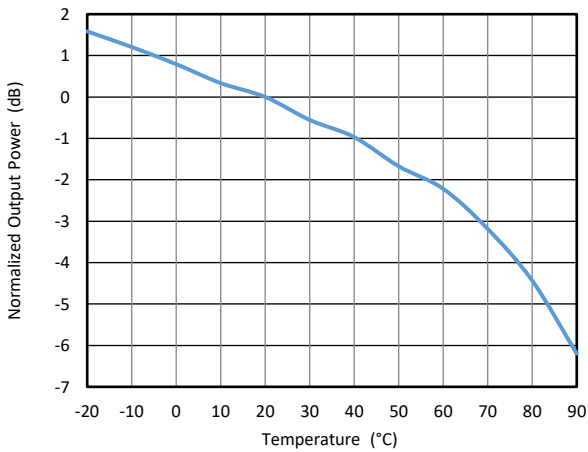


Figure 16 Output Power Swing vs. Temperature (Normalized to 20°C)

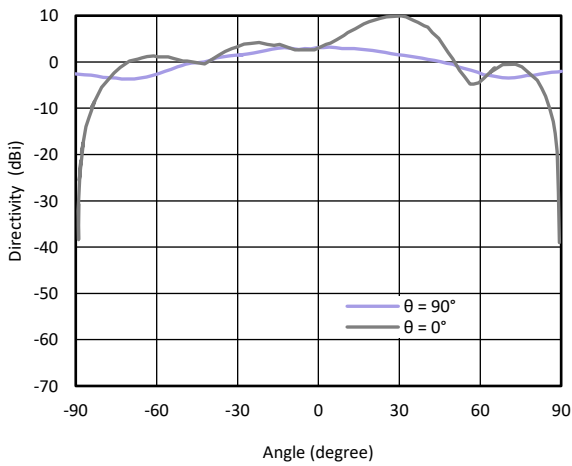


Figure 17 Antenna Radiation Pattern (simulated)

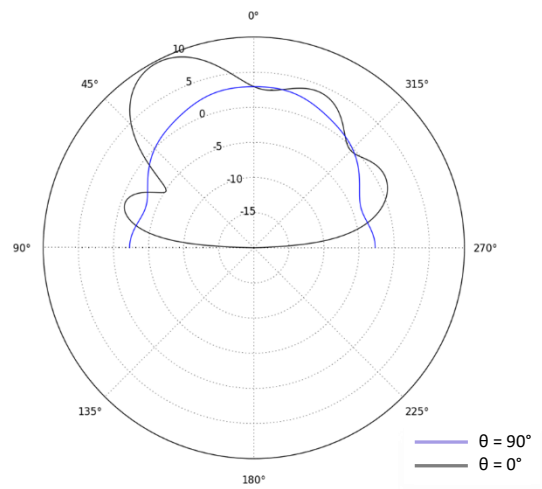


Figure 18 Antenna Radiation Pattern (simulated)

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