BLF0910H9LS750P

Power LDMOS transistor

AMPLEON

Rev. 1 — 22 March 2019

Product data sheet

1. Product profile

1.1 General description

A 750 W LDMOS power transistor for industrial applications at frequency of 915 MHz.

The BLF0910H9LS750P is designed for high-power CW applications and is assembled in a high performance ceramic package.

Table 1. Typical performance

RF performance at V_{DS} = 50 V; I_{Dq} = 50 mA per section in a class-AB application circuit.

Test signal	f	V _{DS}	P_L	G _p	η_{D}
	(MHz)	(V)	(W)	(dB)	(%)
CW [1]	915	50	750	21.5	72.5
CW [2]	902 to 928	50	800	21	69
CW pulsed [3]	915	50	850	21.3	70

^[1] Narrowband circuit.

1.2 Features and benefits

- High efficiency
- Easy power control
- Excellent ruggedness
- Integrated ESD protection
- Designed for broadband operation (902 MHz to 928 MHz)
- Internally input matched
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial applications in the 915 MHz ISM band
- Professional applications in the 915 MHz ISM band

^[2] Broadband circuit.

^[3] Broadband circuit: $t_p = 100 \mu s$; $\delta = 10 \%$; $t_r = 150 ns$; $t_f = 150 ns$.

2. Pinning information

Table 2. Pinning

Description	Simplified outline	Graphic symbol
drain1		
drain2	1 2	1
gate1	5	
gate2	3 4	3 - 5
source	[1]	4
		' ⊢ ¬
		2 sym117
	drain1 drain2 gate1 gate2	drain1 drain2 gate1 gate2

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	Package			
	Name	Description	Version		
BLF0910H9LS750P	-	earless flanged balanced ceramic package; 4 leads	SOT539B		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
V_{DS}	drain-source voltage	-	108	V
V_{GS}	gate-source voltage	-6	+11	V
T _{stg}	storage temperature	-65	+150	°C
Tj	junction temperature [1]	-	225	°C

Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	$T_{case} = 90 ^{\circ}C; P_{L} = 750 W$	0.15	K/W

6. Characteristics

Table 6. DC characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 2.4 \text{ mA}$	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V _{DS} = 10 V; I _D = 240 mA	1.5	2.1	2.5	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	2.8	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	44.5	-	Α
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V	-	-	280	nA
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 8.4 \text{ A}$	-	90	-	mΩ

Table 7. RF characteristics

Test signal: CW pulsed; f = 915 MHz; RF performance at $V_{DS} = 50$ V; $I_{Dq} = 50$ mA per section; $T_{case} = 25$ °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G _p	power gain	P _L = 750 W	20	21.5	-	dB
RLin	input return loss	P _L = 750 W	-	-13	-10	dB
η_{D}	drain efficiency	P _L = 750 W	62.5	65	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF0910H9LS750P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 50 mA per section; P_L = 750 W (CW); tested in band across predefined integer phase steps (narrowband circuit).

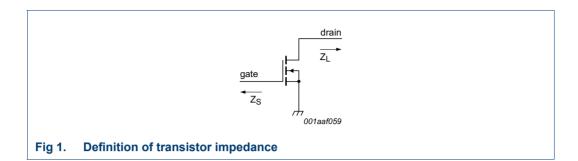
7.2 Impedance information

Table 8. Typical impedance

Measured load-pull Z_S and Z_L device impedances per section; I_{Dq} = 50 mA per section; V_{DS} = 50 V; typical values unless otherwise specified.

f	Z _S [1]	Z _L [1]
(MHz)	(Ω)	(Ω)
915	1.7 – 2.3j	0.9 + 0.7j

[1] Z_S and Z_L defined in Figure 1.



7.3 Test circuit broadband

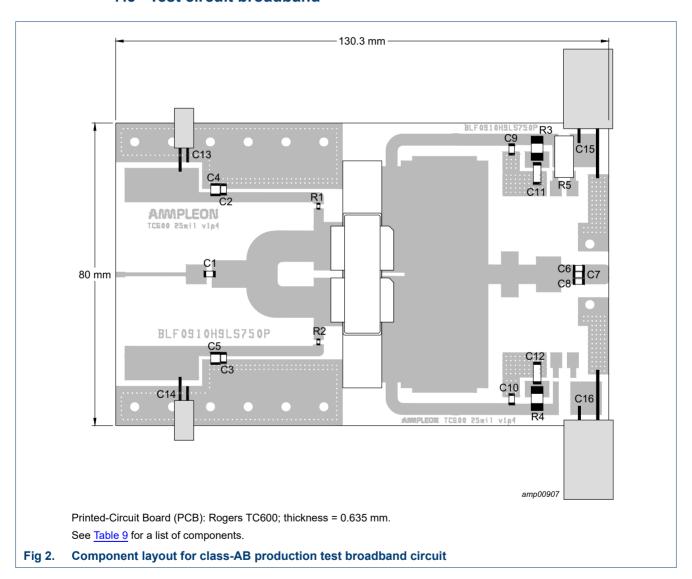


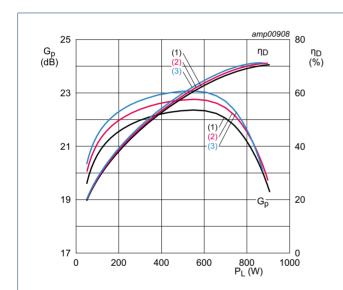
Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C2, C3, C6, C7, C8	multilayer ceramic chip capacitor	560 pF	ATC 800B
C4, C5	multilayer ceramic chip capacitor	1 μF, 50 V	GRM32RR71H105KA01L
C9, C10	multilayer ceramic chip capacitor	47 pF	ATC 100B
C11, C12	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: C5750X7R2A475KT/A
C13, C14	electrolytic capacitor	10 μF, 63 V	
C15, C16	electrolytic capacitor	470 μF, 63 V	
R1, R2	chip resistor	10 Ω	SMD806
R3, R4	chip resistor	3.3 Ω	Bourns: CRS2512
R5	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER

7.4 Graphical data broadband circuit

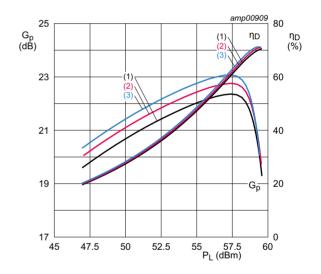
7.4.1 CW



 V_{DS} = 50 V; I_{Dq} = 50 mA per section.

- (1) f = 902 MHz
- (2) f = 915 MHz
- (3) f = 928 MHz

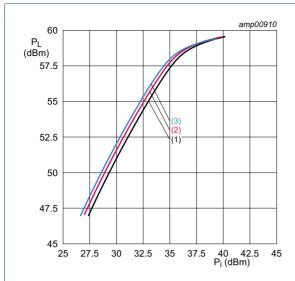
Fig 3. Power gain and drain efficiency as function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 50 mA per section.

- (1) f = 902 MHz
- (2) f = 915 MHz
- (3) f = 928 MHz

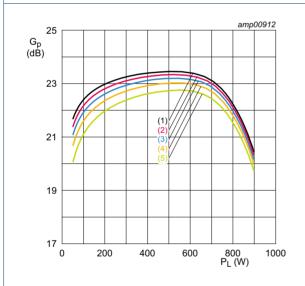
Fig 4. Power gain and drain efficiency as function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 50 mA per section.

- (1) f = 902 MHz
- (2) f = 915 MHz
- (3) f = 928 MHz

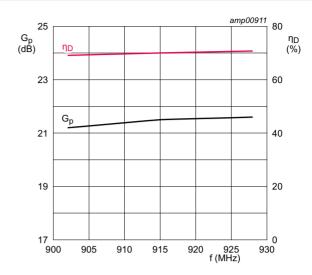
Fig 5. Output power as a function of input power; typical values



 $V_{DS} = 50 \text{ V}$; f = 915 MHz.

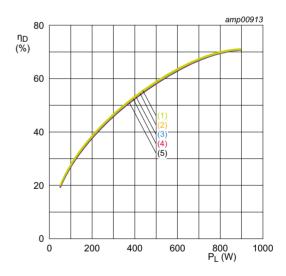
- (1) $I_{Dq} = 250 \text{ mA per section}$
- (2) $I_{Dq} = 200 \text{ mA per section}$
- (3) $I_{Dq} = 150 \text{ mA per section}$
- (4) I_{Dq} = 100 mA per section
- (5) $I_{Dq} = 50 \text{ mA per section}$

Fig 7. Power gain as a function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 50 mA per section; P_L = 800 W.

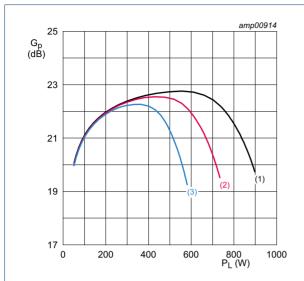
Fig 6. Power gain and drain efficiency as function of frequency; typical values



 $V_{DS} = 50 \text{ V}; f = 915 \text{ MHz}.$

- (1) $I_{Dq} = 250 \text{ mA per section}$
- (2) $I_{Dq} = 200 \text{ mA per section}$
- (3) $I_{Dq} = 150 \text{ mA per section}$
- (4) $I_{Dq} = 100 \text{ mA per section}$
- (5) $I_{Dq} = 50 \text{ mA per section}$

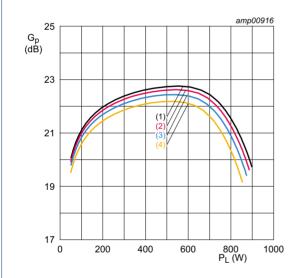
Fig 8. Drain efficiency as a function of output power; typical values



 I_{Dq} = 50 mA per section; f = 915 MHz.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$

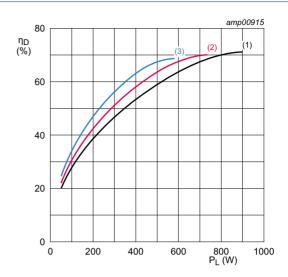
Fig 9. Power gain as a function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 50 mA per section; f = 915 MHz.

- (1) T = 25 °C
- (2) T = 35 °C
- (3) $T = 45 \, ^{\circ}C$
- (4) T = 55 °C

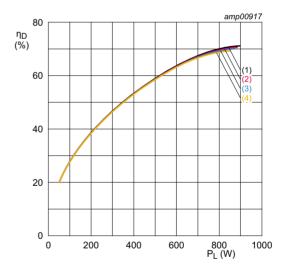
Fig 11. Power gain as a function of output power; typical values



 I_{Dq} = 50 mA per section; f = 915 MHz.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$

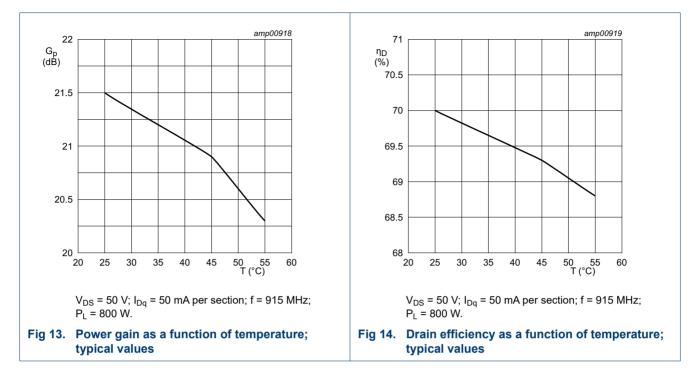
Fig 10. Drain efficiency as a function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 50 mA per section; f = 915 MHz.

- (1) T = 25 °C
- (2) T = 35 °C
- (3) $T = 45 \,^{\circ}C$
- (4) $T = 55 \,^{\circ}C$

Fig 12. Drain efficiency as a function of output power; typical values



7.5 Test circuit narrowband

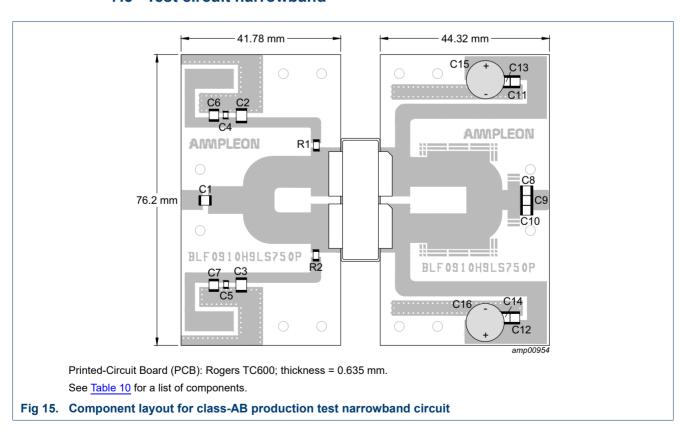


Table 10. List of components

For test circuit see Figure 15.

Component	Description	Value	Remarks
C1, C2, C3, C8, C9, C10, C11, C12	multilayer ceramic chip capacitor	47 pF	ATC 100B
C4, C5, C13, C14	multilayer ceramic chip capacitor	1 '	Multicomp: MCMT21N02F101CT
C6, C7	multilayer ceramic chip capacitor	1 μF, 50 V	GRM32RR71H105KA01L
C15, C16	electrolytic capacitor	470 μF, 63 V	
R1, R2	chip resistor	10 Ω	SMD1206

7.6 Graphical data narrowband circuit

7.6.1 CW

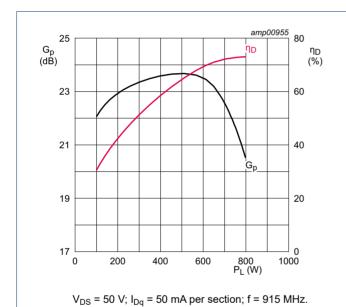
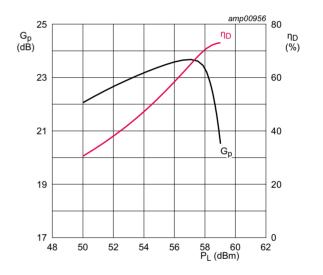


Fig 16. Power gain and drain efficiency as function of output power; typical values



 V_{DS} = 50 V; I_{Dq} = 50 mA per section; f = 915 MHz.

Fig 17. Power gain and drain efficiency as function of output power; typical values

8. Package outline

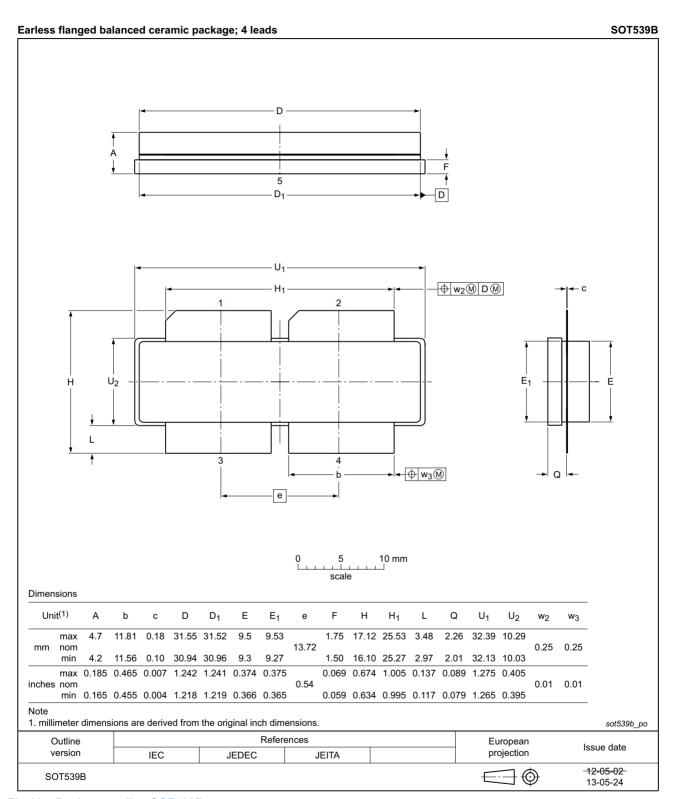


Fig 18. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

- [1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.
- [2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF0910H9LS750P v.1	20190322	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Power LDMOS transistor

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13. Contact information

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