

Silicon Radar GmbH Im Technologiepark 1 15236 Frankfurt (Oder) Germany

fon +49.335.557 17 74 fax +49.335.557 10 50 https://www.siliconradar.com

TRX_024_006

24-GHz Highly Integrated IQ Transceiver

Data Sheet

Status:	Date:	Author:	Filename:	
Final	2018-09-28	Silicon Radar GmbH	Datasheet_TRX_024_006_V2.1	
Version:	Product number:	Package:	Marking:	Page:
2.1	TRX_024_006	QFN20, 3×3 mm ²	TRX006 YYWW	1 of 16



Version Control

Version	Changed section	Description of change	Reason for change
1.6	Product name	Changed from TRX_024_06 to TRX_024_006	New procedure for product nomenclature
	Status	From preliminary to final	Product released to serial production
	Max Ratings	ESD integrity updated	New test results
1.7	Specification	Spec data revised	Routinely revision
1.8	Package Dimensions	IC weight added	Customer request
1.9	Specification	IQ imbalance and thermal resistance values changed	Correction
2.0	Overview	Typos fixed	Routinely revision
	Electrical Characteristics	Level of logic input specified	Correction
	Measurements Results	Diagram TX power vs. Temperature added Description of analog behavior of inputs d0 – d3 added	New test results
2.1	3.2 Pin Description	Table 1: LNA-gain control input voltage corrected	Correction
	6.2 Power Cycling	Application hint added	Update
	6.4 Evaluation Kit	Reference to Silicon Radar's evaluation kit SiRad Easy®	Update
	7 Meas. Results	Figure 10: Name of x-axis corrected, Figure 12: Name of data series corrected	Correction



Table of Contents

1	Features	4
1.1	Overview	Δ
1.2	Applications	Δ
2	Block Diagram	5
3	Pin Configuration	5
3.1	Pin Assignment	
3.2	Pin Description	
4	Specification	
4.1	Absolute Maximum Ratings	
4.2	Operating Range	
4.3	Thermal Resistance	
4.4	Electrical Characteristics	8
5	Packaging	<u>c</u>
5.1	Package Dimensions	
5.2	Package Footprint	
5.3	Package Code	10
5.4	Qualification Test	10
6	Application	11
6.1	Application Circuit Schematic	
6.2	Power Cycling	11
6.3	Evaluation Board	12
6.4	Evaluation Kit	12
6.5	Input / Output Stages	13
7	Measurement Results	14



1 Features

- Radar transceiver for 24-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 300 mW in continuous operating mode
- Transmitter with power control in two steps
- Receiver with homodyne quadrature mixers
- Low-noise amplifier (LNA) with gain control
- Integrated low phase noise push-push VCO
- Divider division ratio 1:32 (1:8 available in TRX_024_007)
- Single ended TX output
- Single ended RX input
- QFN20 leadless plastic package 3 × 3 mm²
- Pb-free, RoHS compliant package
- IC is available as bare die as well



1.1 Overview

The IC is an integrated transceiver circuit for the 24-GHz ISM band in the frequency range $24.0\,\text{GHz} - 24.25\,\text{GHz}$. It includes a low-noise amplifier (LNA) with gain control, quadrature mixers, a poly-phase filter, a voltage controlled oscillator with band switching and a divide-by-32 circuit. The transmitter can be powered down if TX_EN pin is supplied with 0 V. The gain of the receiver can be digitally controlled by Vct pin: Vct = $3.3\,\text{V}$ sets the receiver in high gain mode, Vct = $0\,\text{V}$ sets the receiver in low gain mode. The output power of the transmitter can be controlled by the pwr1 input. The IC is fabricated in SiGe BiCMOS technology.

Beside the TRX_024_006, an IC variant with a divider division ratio of 1:8 is available as TRX_024_007.

1.2 **Applications**

The TRX_024_006 can be used in wireless communication systems and in radar systems for the ISM band from 24.0 GHz to 24.25 GHz and for UWB applications between 23 GHz and 26 GHz.



2 Block Diagram

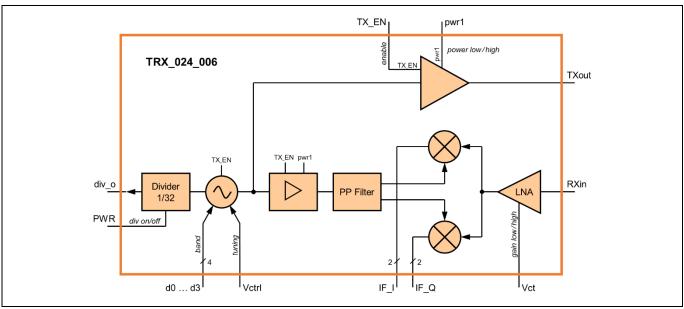


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

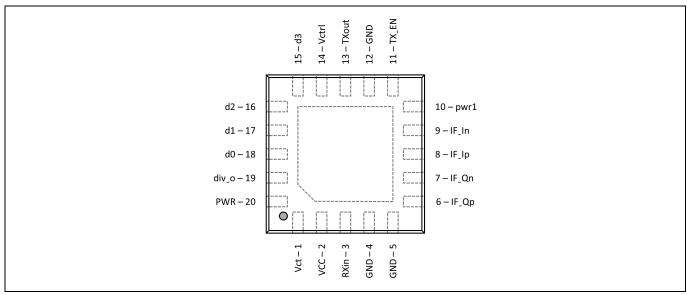


Figure 2 Pin Assignment (QFN20, Top View)



3.2 <u>Pin Description</u>

Table 1 Pin Description

Pin		Description
No.	Name	
1	Vct	LNA gain control input, with internal 100-k Ω pull-up resistor: 3.3 V – high gain mode, 0 – low gain mode
2	VCC	Supply voltage
3	RXin	RF input, 50Ω
4, 5	GND	Ground
6	IF_Qp	
7	IF_Qn	IS autoute DC coupled automat AC coupling consistent according
8	IF_lp	IF outputs, DC coupled, external AC coupling capacitors required
9	IF_In	
10	pwr1	Power-amplifier gain control input with internal 100-k Ω pull-up resistor: 3.3 V – P_{OUT_MAX} , 0 – P_{OUT_MAX} - 4 dB
11	TX_EN	TX enable input, high active, with internal 100-kΩ pull-up resistor: 3.3 V – enable, 0 – off
12	GND	Ground
13	TXout	Transmitter output, 50Ω
14	Vctrl	VCO tuning voltage input
15	d3	
16	d2	VCO hand suitables in auto-sable mutuith internal 420 bo will decomposite.
17	d1	VCO band switching inputs, each input with internal 120-kΩ pull-down resistor
18	d0	
19	div_o	Divider output, 50 Ω, DC coupled, external decoupling capacitor required (min. 100 pF)
20	PWR	Divider enable input, with internal 100-kΩ pull-up resistor: 3.3 V – enable, 0 – off
(21)	GND	Exposed die attach pad of the QFN package, must be soldered to ground



4 Specification

4.1 <u>Absolute Maximum Ratings</u>

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only given within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply voltage	V _{CC}		3.6	V	to GND
DC voltage at RF pins	V_{DCRF}	0	2	mV	IC provides low ohmic circuit to GND for TXout and RXin
Junction temperature	TJ		150	°C	
Storage temperature range	T _{STG}	-65	150	°C	
DC voltage at control inputs	V _{CTL}	-0.3	V _{CC} + 0.3	V	d0, d1, d2, d3, Vctrl, Vct, pwr1, TX_EN, PWR
Input power into pin RFin	P _{IN}		0	dBm	
ESD robustness	V _{ESD}		500	V	Class 1A, Note 1

Note 1 According to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 **Operating Range**

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Ambient temperature	T _A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	>	(3.3V ± 5%)
DC voltage at control inputs	V _{CTL}	0	V _{CC}	V	d0, d1, d2, d3, Vctrl, Vct, pwr1, TX_EN, PWR

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Тур	Max	Unit	Condition / Remark
Thermal resistance, junction-to- ambient	R _{thja}			75	K/W	Four-layer PCB according to JEDEC standard JESD-51



4.4 <u>Electrical Characteristics</u>

 T_A = -40 °C to +85 °C unless otherwise noted. Typical values measured at T_A = 25 °C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

Supply current consumption Icc 80 89 100 mA TX, divider enabled	Table 5 Electrical Characteristics				•		
Supply current consumption Icc 80 89 100 mA TX, divider enabled	Parameter	Symbol	Min	Тур	Max	Unit	Condition / Remark
Control input voltage, low level V _{IN_L} 0 0.3 × V _{CC} V Inputs TX_EN, pwr1, PWR Control input voltage, high level V _{IN_H} 0.7 × V _{CC} Vcc V and Vct Transmitter Section TX Transmitter start frequency f _{TX} 22.3 22.8 23.3 GHz Divider output frequency f _{RIV_O} 700 840 MHz Tuning voltage VCO Vcri 0 3.3 V Tuning voltage VCO Vcri 0 3.3 V Number of adjustable frequency bands 16 220 MHz/V Only Vctrl swept Number of adjustable frequency bands 4 f _{TX} /ΔV _{CC} 135 MHz/V Only Vctrl swept Number of adjustable frequency bands 4 f _{TX} /ΔV _{CC} 135 MHz/V Only Vctrl swept Number of adjustable frequency bands 2 f _{TX} 120 MBc/Hz Divider output power 6 dBc/Hz 11 MHz offset Output impedance P _{TX} 2.5 4 6 dBm AV Output power<	DC Parameters						
Control input voltage, high level V _{IN_IP} 0.7 × V _{CC} V _{CC}	Supply current consumption	I _{CC}	80	89	100	mA	TX, divider enabled
Transmitter Section TX	Control input voltage, low level	V_{IN_L}	0		$0.3 \times V_{CC}$	V	Inputs TX_EN, pwr1, PWR
Transmitter start frequency F _{TX} 22.3 22.8 23.3 GHz	Control input voltage, high level	V _{IN_H}	$0.7 \times V_{CC}$		Vcc	V	and Vct
Transmitter stop frequency	Transmitter Section TX						
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Transmitter start frequency	f_{TX}	22.3	22.8	23.3	GHz	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Transmitter stop frequency		25.9	26.4	26.9	GHz	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Divider division ratio	$D_{div_{o}}$		32			Note 1
Tuning slope VCO (Vctrl)	Divider output frequency	f _{div_o}	700		840	MHz	
Number of adjustable frequency bands 16	Tuning voltage VCO	V_{ctrl}	0		3.3	V	
bands Λοte 1 Pushing VCO Δf _{Tr} /ΔVcc 135 MHz/V f = 24.15 GHz Phase noise P _N -105 -102 dBc/Hz at 1 MHz offset Output impedance Z _{TXout} 50 Ω C Transmitter output power P _{TX} 2.5 4 6 dBm Adjustable range output power P _{TX_ADJ} 0 4 dBm pwr1 = 0 / 3.3 V Divider output power P _{TX_ADJ} 0 4 dBm pwr1 = 0 / 3.3 V Divider output power P _{TX_ADJ} 0 4 dBm pwr1 = 0 / 3.3 V Divider output power P _{TX_ADJ} 0 4 dBm Note 2 Spurious power P _{Sp-} -40 dBm f _{TX} + f _{div} Harmonics power P _{Ha12} -46 dBm 12 GHz Harmonics power f _{RA3} 22.3 26.9 GHz Receiver Section RX Receiver frequency f _{RX} 22.3 26.9 GHz Receiver fre	Tuning slope VCO (Vctrl)	$\Delta f_{TX}/\Delta V_{ctrl}$		220		MHz/V	Only Vctrl swept
Phase noise P _N -105 -102 dBc/Hz at 1 MHz offset Output impedance Z _{TXout} 50 Ω Transmitter output power P _{TX} 2.5 4 6 dBm Adjustable range output power P _{TX_ADJ} 0 4 dBm pwr1 = 0 / 3.3 V Divider output power P _{div_0} -9 -8.5 -8 dBm Note 2 Spurious power P _{Sp} -40 dBm f _{TX} - f _{div} Harmonics power P _{Ha12} -46 dBm 12 GHz P _{Ha48} -40 dBm 48 GHz Receiver Section RX Receiver frequency f _{RX} 22.3 26.9 GHz Receiver input impedance Z _{RXIN} 50 Ω Ω Number of adjustable gain modes 2 Adjustable LNA gain control Gain high gain mode 18 dB V _{ct} = 3.3 V Gain low gain mode 11 dB V _{ct} = 0 IF requency range f _{IF} 0	Number of adjustable frequency bands			16			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		135		MHz/V	f = 24.15 GHz
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Phase noise	P _N	-105	-102		dBc/Hz	at 1 MHz offset
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Output impedance	Z _{TXout}		50		Ω	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Transmitter output power	P _{TX}	2.5	4	6	dBm	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Adjustable range output power	P _{TX_ADJ}	0		4	dBm	pwr1 = 0 / 3.3 V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Divider output power	P _{div_o}	-9	-8.5	-8	dBm	Note 2
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Spurious power	P _{Sp-}		-40		dBm	f _{TX} - f _{div}
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		P _{Sp+}		-43		dBm	$f_{TX} + f_{div}$
Receiver Section RXReceiver frequency f_{RX} 22.3 26.9 GHz Receiver input impedance Z_{RXIN} 50 Ω Number of adjustable gain modes 2 Adjustable LNA gain controlGain high gain mode 18 dB $V_{ct} = 3.3 \text{ V}$ Gain low gain mode 11 dB $V_{ct} = 0$ IF frequency range f_{IF} 0 200 MHz IF output impedance Z_{OUT} 470 Ω Ω IQ amplitude imbalance -1 1 dB IQ phase imbalance -10 10 deg Noise figure, high gain mode 4 dB SimulatedNoise figure, low gain mode 6 dB Gouble side band at $f_{IF} = 1 \text{ MHz}$	Harmonics power	P _{Ha12}		-46		dBm	12 GHz
Receiver frequency f_{RX} 22.326.9GHzReceiver input impedance Z_{RXIN} 50 Ω Number of adjustable gain modes2Adjustable LNA gain controlGain high gain mode18dB $V_{ct} = 3.3 \text{ V}$ Gain low gain mode11dB $V_{ct} = 0$ IF frequency range f_{IF} 0200MHzIF output impedance Z_{OUT} 470 Ω DifferentialIQ amplitude imbalance-11dBIQ phase imbalance-1010degNoise figure, high gain mode4dBSimulatedNoise figure, low gain mode6dB(double side band at $f_{IF} = 1 \text{ MHz}$)		P _{Ha48}		-40		dBm	48 GHz
Receiver input impedance Z_{RXIN} 50 Ω Number of adjustable gain modes 2 Adjustable LNA gain control Gain high gain mode 18 dB $V_{ct} = 3.3 \text{ V}$ Gain low gain mode 11 dB $V_{ct} = 0$ IF frequency range f_{IF} 0 200 MHz IF output impedance Z_{OUT} 470 Ω Differential IQ amplitude imbalance -1 1 dB IQ phase imbalance -10 10 deg Noise figure, high gain mode 4 dB Simulated Noise figure, low gain mode 6 dB (double side band at $f_{IF} = 1 \text{ MHz}$)	Receiver Section RX						
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Receiver frequency	f_{RX}	22.3		26.9	GHz	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Receiver input impedance	Z _{RXIN}		50		Ω	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Number of adjustable gain modes			2			Adjustable LNA gain control
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gain high gain mode				18	dB	V _{ct} = 3.3 V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Gain low gain mode				11	dB	V _{ct} = 0
IQ amplitude imbalance -1 1 dB IQ phase imbalance -10 10 deg Noise figure, high gain mode 4 dB Simulated Noise figure, low gain mode 6 dB (double side band at f _{IF} = 1 MHz)	IF frequency range	f_{IF}	0		200	MHz	
IQ phase imbalance-1010degNoise figure, high gain mode4dBSimulatedNoise figure, low gain mode6dB(double side band at $f_{IF} = 1 \text{ MHz}$)	IF output impedance	Z _{OUT}		470		Ω	Differential
Noise figure, high gain mode 4 dB Simulated Noise figure, low gain mode 6 dB (double side band at $f_{\rm IF}$ = 1 MHz)	IQ amplitude imbalance		-1		1	dB	
Noise figure, low gain mode $\frac{1}{2}$ 6 dB (double side band at $f_{IF} = 1$ MHz)	IQ phase imbalance		-10		10	deg	
	Noise figure, high gain mode			4		dB	Simulated
Input compression point 1dB ICP -20 -13 dBm	Noise figure, low gain mode			6		dB	(double side band at $f_{IF} = 1 \text{ MHz}$)
	Input compression point	1dB ICP	-20		-13	dBm	

Note 1 See also chapter "Measurement Results", Figure 10 and 11.

Note 2 Divider output is loaded with 50 Ω , DC coupled, external decoupling capacitor \geq 100 pF required.



5 Packaging

5.1 Package Dimensions

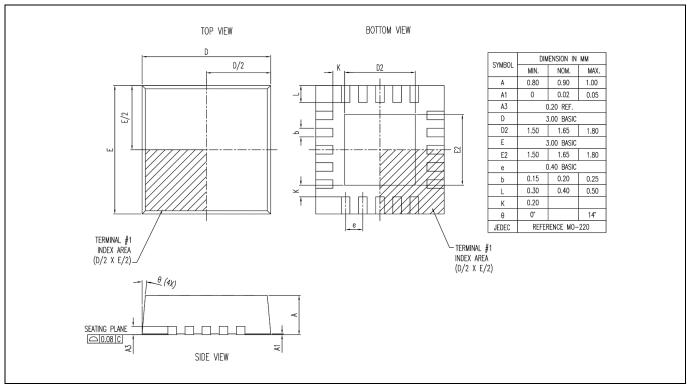


Figure 3 Outline Dimensions of QFN20, 3 × 3 mm², 0.4 mm Pitch

IC Weight: 0.235 g (typ.)

5.2 <u>Package Footprint</u>

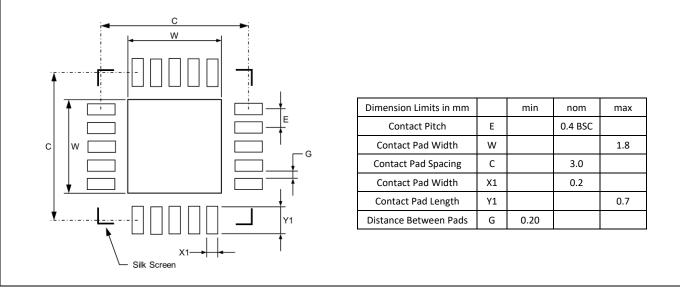


Figure 4 Recommended Land Pattern



5.3 Package Code

Top-Side Markings TRX006 YYWW

5.4 **Qualification Test**

Table 6 Reliability and Environmental Test

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	pass

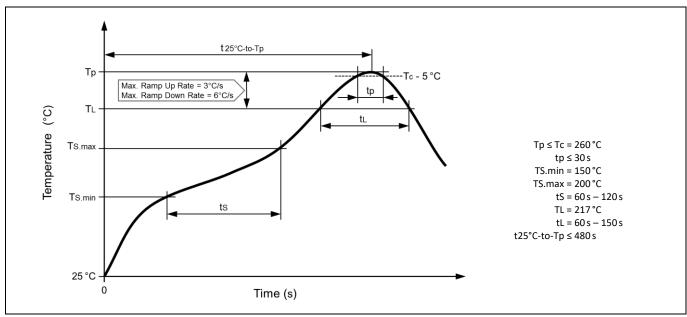


Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E



6 Application

6.1 Application Circuit Schematic

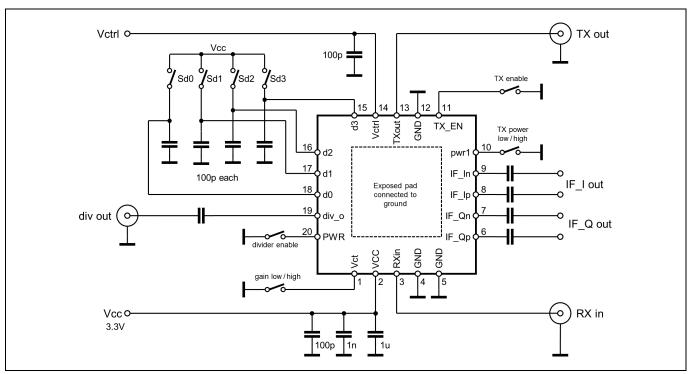


Figure 6 Application Circuit for Band Switching

6.2 **Power Cycling**

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and $100\,\mu s$ is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.



6.3 <u>Evaluation Board</u>

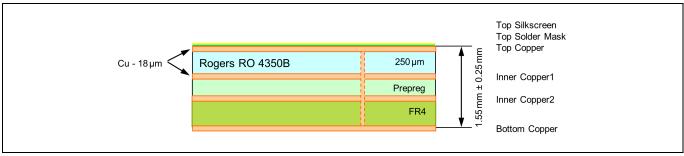


Figure 7 Evaluation Board Stack-up

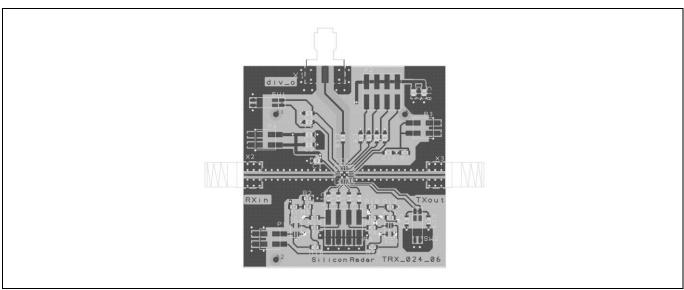


Figure 8 Evaluation Board Layout Including Via Holes (50 mm × 50 mm, Top View)

6.4 <u>Evaluation Kit</u>

For a quick and easy start into radar development Silicon Radar offers SiRad Easy[®]. It is an evaluation board system for many of our integrated IQ transceivers with antennas in package or on PCB. It comes with a reference hardware and provides a complete design environment which can be configured via a browser-based graphical interface. Its rich functionality and the open communication protocol make it a versatile tool – also for enhanced development projects.

It features:

- Distance measurement
- Velocity measurement
- Frequency modulated continuous wave mode (FMCW)
- Continuous wave mode (CW)

For more information about the features of SiRad Easy® see:

https://www.siliconradar.com/evalkits_e.html



6.5 <u>Input / Output Stages</u>

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

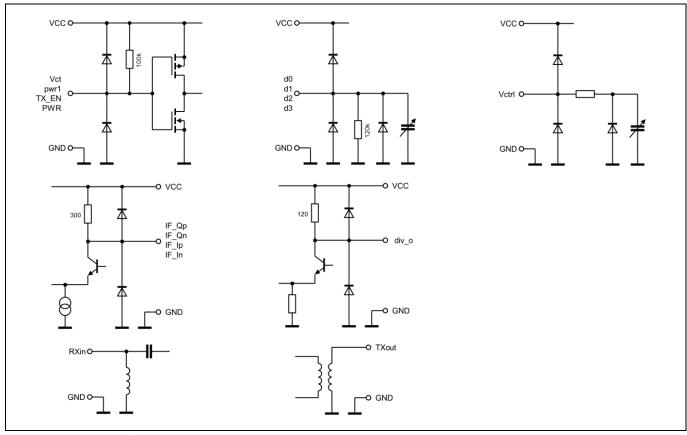


Figure 9 Equivalent I/O Circuits



7 Measurement Results

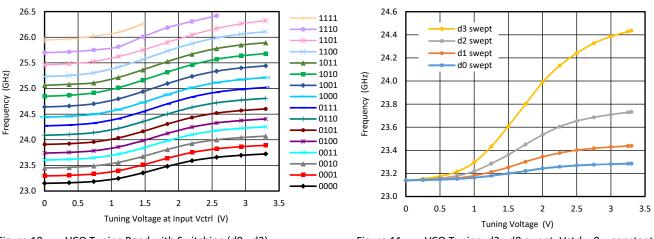


Figure 10 VCO Tuning Band with Switching (d0 - d3)

Figure 11 VCO Tuning, d3 - d0 swept, Vctrl = 0 = constant

VCO band switching inputs d3 to d0 can be used to switch the output frequency band as in Figure 10. As an example, input combination "0101" with d3, d1 = 3.3 V and d2, d0 = 0 includes the 24-GHz ISM band. However, the designer should take into account that output frequency bands may shift from chip to chip (see Figure 12), and same switch settings may not give the same output band.

Note, VCO band switching inputs d0 - d3 are analog inputs and can be used to control the output frequency. The bandwidth of the switching inputs increases from d0 to d3. Any of these pins can be interconnected to each other and/or to pin Vctrl to use different bandwidth capabilities of the VCO.

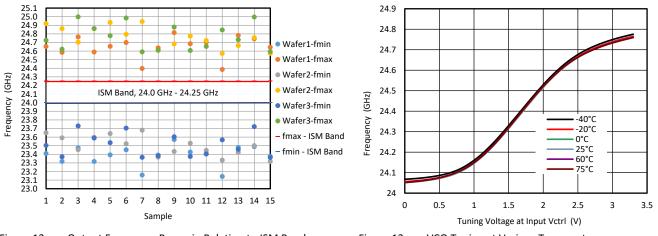


Figure 12 Output Frequency Range in Relation to ISM Band for Several Chips (f_{min}, f_{max} measurement)

Figure 13 VCO Tuning at Various Temperatures (tuning voltage Vctrl)

The input settings for the measurement shown in Figure 12 are d3 = 0 (0 V), d2 = 1 (3.3 V). Inputs d0, d1, and Vctrl are interconnected and swept together.



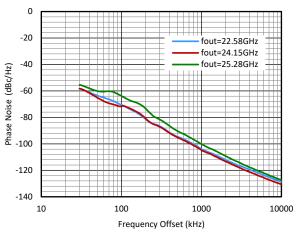


Figure 14 Phase Noise of the Free-Running VCO

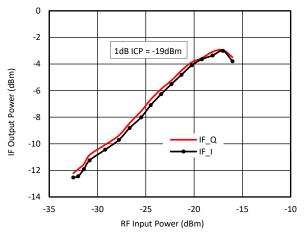


Figure 16 Conversion Gain of the Receiver in High-Gain Mode

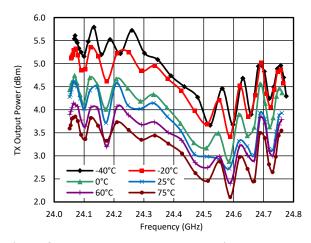


Figure 18 TX Power vs. Frequency at Various Temperatures

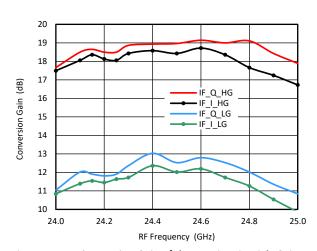


Figure 15 Conversion Gain of the Receiver in High-Gain and Low-Gain Mode

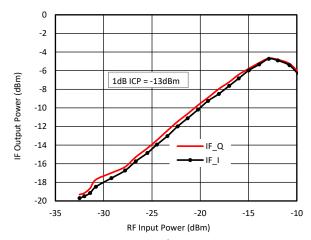


Figure 17 Conversion Gain of the Receiver in Low-Gain Mode



Disclaimer

Silicon Radar GmbH 2018. The information contained herein is subject to change at any time without notice.

Silicon Radar GmbH assumes no responsibility or liability for any loss, damage or defect of a product which is caused in whole or in part by

- (i) use of any circuitry other than circuitry embodied in a Silicon Radar GmbH product,
- (ii) misuse or abuse including static discharge, neglect, or accident,
- (iii) unauthorized modifications or repairs which have been soldered or altered during assembly and are not capable of being tested by Silicon Radar GmbH under its normal test conditions, or
- (iv) improper installation, storage, handling, warehousing, or transportation, or
- (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: Silicon Radar GmbH makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any Silicon Radar product and any product documentation. Products sold by Silicon Radar are not suitable or intended to be used in a life support applications or components, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY: BUYER AGREES NOT TO USE SILICON RADAR GMBH'S PRODUCTS FOR ANY APPLICATIONS OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

Silicon Radar GmbH owns all rights, titles and interests to the intellectual property related to Silicon Radar GmbH's products, including any software, firmware, copyright, patent, or trademark. The sale of Silicon Radar GmbH's products does not convey or imply any license under patent or other rights. Silicon Radar GmbH retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by Silicon Radar GmbH. Unless otherwise agreed to in writing by Silicon Radar GmbH, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.