Silicon Radar GmbH
Im Technologiepark 1
15236 Frankfurt (Oder)
Germany

fon +49.335.557 17 74
fax +49.335.557 10 50
https://www.siliconradar.com

TRX_120_001

120-GHz Highly Integrated IQ Transceiver with Antennas in Package
in Silicon Germanium Technology

Data Sheet

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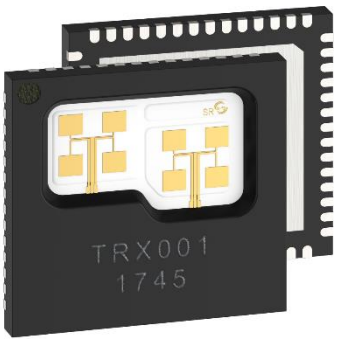
Version:	Product number:	Package:	Marking:	Page:
1.4	TRX_120_001	QFN56, 8 × 8 mm²	TRX001 YYWW	1 of 16

Version Control

Version	Changed section	Description of change	Reason for change
0.6	template	added sections version control and document release	controlled document
0.7	pin configuration	revised	routinely revision
1.0	ratings, figures, measurement results	added section 'Reliability… ', revised section 'Application'	finalize document
1.1	block diagram	typo fixed	routinely revision
1.2	figure 4: Antenna Position	pin assignment corrected	correction
1.3	3.2 Pin description 6.2 Power Cycling	pin 17 , pwr_tx is renamed to control input (instead of enable input) Application hint added	correction update
1.4	1 Features	package depiction updated	routinely revision

Table of Contents

1 Features



- Radar front end (RFE) with antennas in package for 122-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 380 mW
  in continuous operating mode
- Duty cycling possible
- Integrated low phase noise push-push VCO
- Receiver with homodyne quadrature mixer
- RX and TX patch antennas
- Wide bandwidth of up to 7 GHz
- QFN56 leadless plastic package 8 × 8 mm²
- Package partly molded, MSL3 rated
- Pb-free, RoHS compliant package
- IC is available as bare die as well (without antennas)

1.1 Overview

The RFE is an integrated transceiver circuit for the 122-GHz ISM band with antennas in package. It includes a low-noise amplifier (LNA), quadrature mixers, a poly-phase filter, a voltage controlled oscillator, divide-by-32 outputs and transmit and receive antennas (see Figure 1). The RF signal from the oscillator is directed to the RX path via buffer circuits. The RX signal is amplified by the LNA and converted to baseband by two mixers with quadrature local oscillator (LO). The 120-GHz LO has four analog tuning inputs with different tuning ranges and tuning slopes. The tuning inputs can be combined to obtain a wide frequency tuning range. The analog tuning inputs together with integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing analog tuning inputs.
The IC is fabricated in SG13S SiGe BiCMOS technology of IHP GmbH.

1.2 Applications

The main field of application for the 120-GHz transceiver radar frontend is in short range radar systems with a range up to about 10 meters. By using dielectric lenses, the range can be increased considerably. The RFE can be used in FMCW mode as well as in CW mode. Although the chip is intended for use in the ISM band 122 GHz - 123 GHz, it is also possible to extend the bandwidth to the full tuning range of 7 GHz.

2 Block Diagram

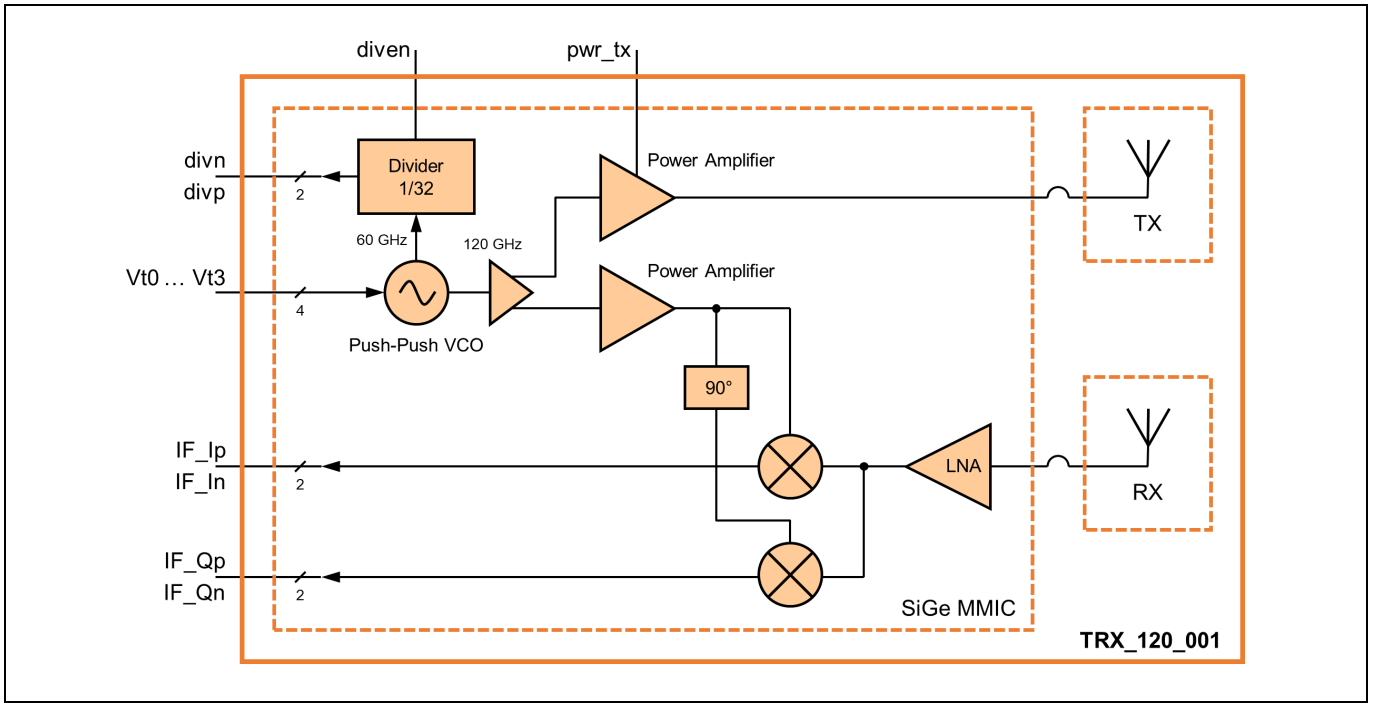


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

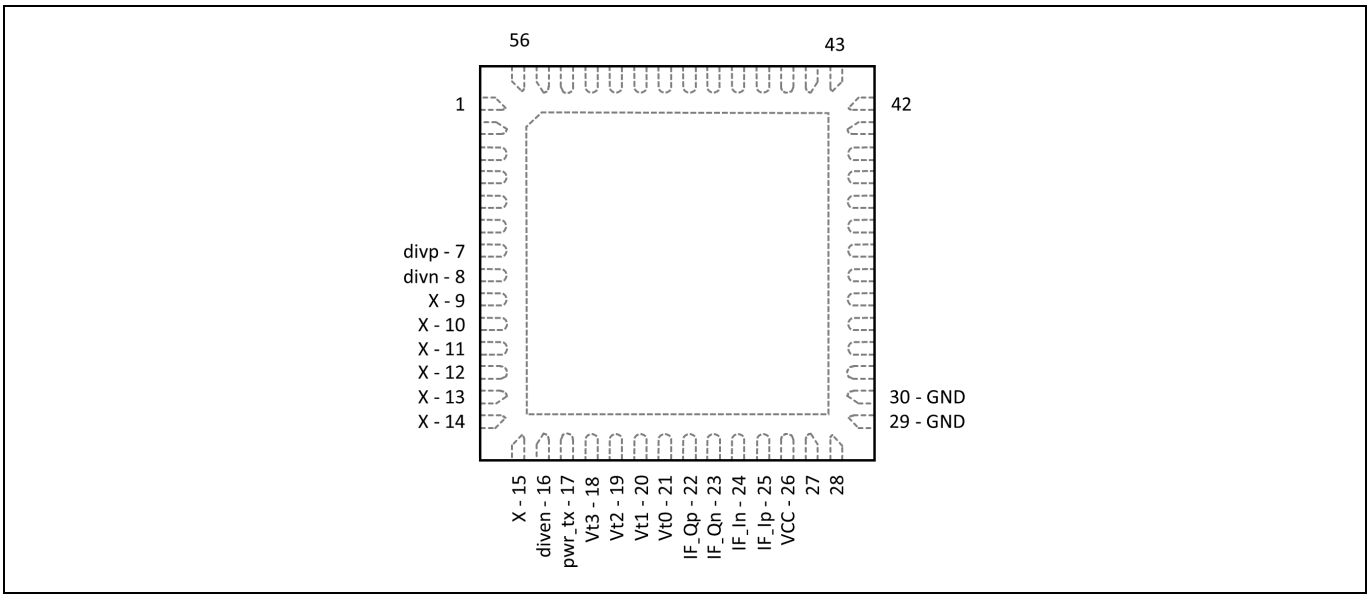


Figure 2 Pin assignment (QFN56, top view)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
1 - 6	NC	Not connected
7	divp	Divider output, 50 Ω, DC coupled, external decoupling capacitor required.
8	divn	Divider output, 50 Ω, DC coupled, external decoupling capacitor required.
9 - 15	X	Reserved. Do not make any connections.
16	diven	Divider enable input (enable = 1.2 V, off = 0), NMOS input, external pull-up resistor of 100 kΩ recommended.
17	pwr_tx	Transmitter power control input (normal = 1.2 V, -3 dB = 0), NMOS input, external pull-up resistor of 100 kΩ recommended.
18	Vt3	VCO tuning input 3 (0 – V_{CC})
19	Vt2	VCO tuning input 2 (0 – V_{CC})
20	Vt1	VCO tuning input 1 (0 – V_{CC})
21	Vt0	VCO tuning input 0 (0 – V_{CC})
22	IF_Qp	IF Q output, positive terminal (DC coupled)
23	IF_Qn	IF Q output, negative terminal (DC coupled)
24	IF_In	IF I output, negative terminal (DC coupled)
25	IF_Ip	IF I output, positive terminal (DC coupled)
26	VCC	Supply voltage (3.3 V, 112 mA typ.)
27, 28	NC	Not connected
29, 30	GND	Ground pins, also connected to the exposed die attach pad.
31 - 56	NC	Not connected
(57)	GND	Exposed die attach pad of the QFN package, must be soldered to ground.

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Supply voltage	V_{CC}		3.6	V	to GND
DC voltage at tuning inputs	V_{Vt}	-0.3	V_{CC} + 0.3	V	Inputs Vt0, Vt1, Vt2, Vt3
DC voltage at enable inputs	V_{EN}	-0.3	1.5	V	Inputs diven, pwr_tx
Junction temperature	T_J	-50	150	°C	
Storage temperature range	T_{STG}		150	°C	
Floor life (out of bag) at factory ambient (30°C / 60% RH)	FL		168	h	IPC/JEDEC J–STD-033A MSL Level 3 Compliant [1)]
ESD robustness	V_{ESD}		500	V	Human body model, HBM [2)]

1) If the devices are stored outside of the packaging, beyond this time limit, the device should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 12 hours.
2) CLASS 1A according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning inputs	V_{Vt}	0	V_{CC}	V	Inputs Vt0 – Vt3
DC voltage at enable inputs	V_{EN}	0	1.2	V	Inputs diven, pwr_tx

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R_{thja}			30	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

T_A = -40°C to +85°C unless otherwise noted. Typical values measured at T_A = 25°C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
DC Parameters						
Supply current consumption	I_{CC}		112	125	mA	TX on, CW mode
Enable input voltage, low level	V_{EN_L}	0		0.3	V	Inputs diven, pwr_tx
Enable input voltage, high level	V_{EN_H}	0.9		1.2	V	Inputs diven, pwr_tx
VCO tuning voltage	V_{Vt}	0		V_{CC}	V	Inputs Vt0 – Vt3
RF Parameters						
VCO start frequency	f_{TX}	117.8	119.3	120.8	GHz	Vt0 = Vt1 = Vt2 = Vt3 = 0
VCO stop frequency	f_{TX}	124.3	125.8	127.3	GHz	Vt0 = Vt1 = Vt2 = Vt3 = 3.3 V
VCO tuning full bandwidth	Δf_{TX}	5.5	6.5	7.5	GHz	Vt0 – Vt3 interconnected
Number of adjustable frequency bands			8			Vt1 – Vt3 used for band switching
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		27		MHz/V	
Phase noise	P_N		-90	-88	dBc/Hz	at 1 MHz offset
Transmitter output power	P_{TX}	-7	-3	1	dBm	Measured without antennas, V(pwr_tx) = 1.2 V
Divider ratio of TX signal	N_{div}		64			
Divider output power	P_{div}	-10		-7	dBm	Note 1
Divider output frequency	f_{div}	1.84		1.99	GHz	
Receiver gain			8	10	dB	Measured without antennas
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		500		Ω	Differential outputs
IQ amplitude imbalance			3		dB	
IQ phase imbalance		-10		10	deg	
Noise figure (DSB)			8.7		dB	Simulated, at f_{IF} = 1 MHz
Input compression point	1dB ICP		-20		dBm	Measured without antennas

Note 1: Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.

5 Packaging

5.1 Outline Dimensions

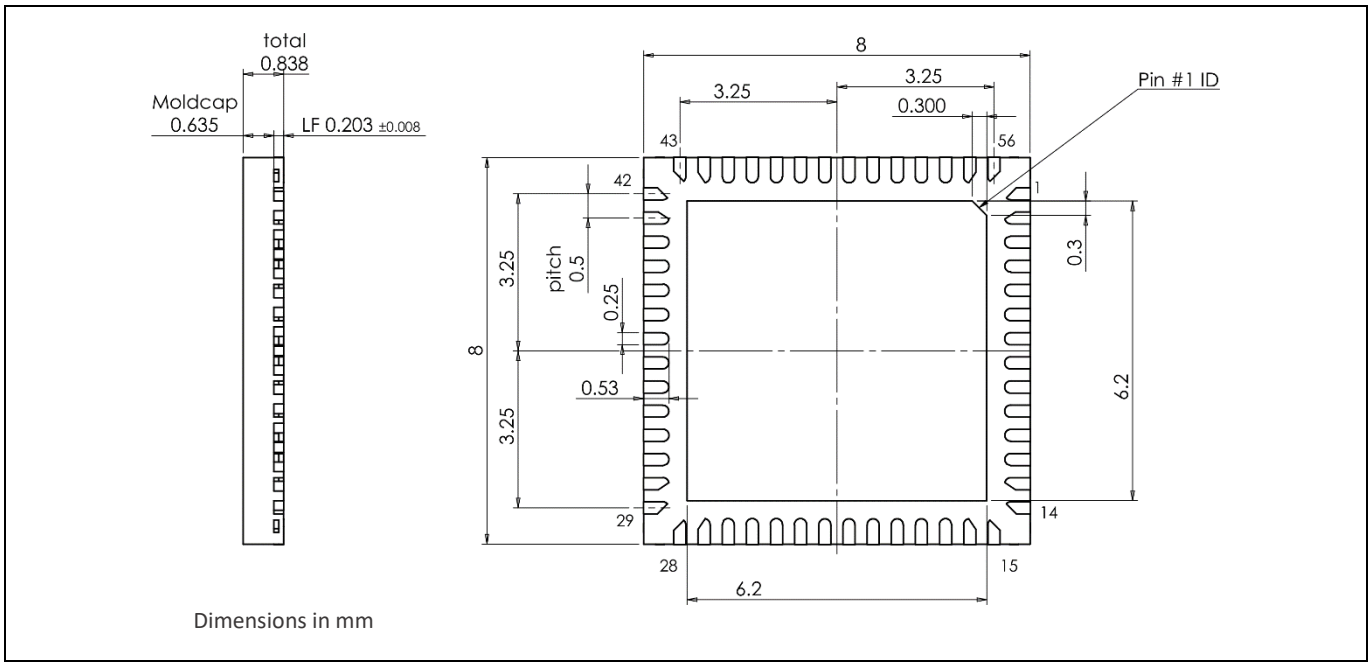


Figure 3 Outline Dimensions of QFN56, 0.5 mm Pitch, 8 mm × 8 mm

5.2 Package Code

Top-Side Markings	TRX001 YYWW

5.3 Antenna Position

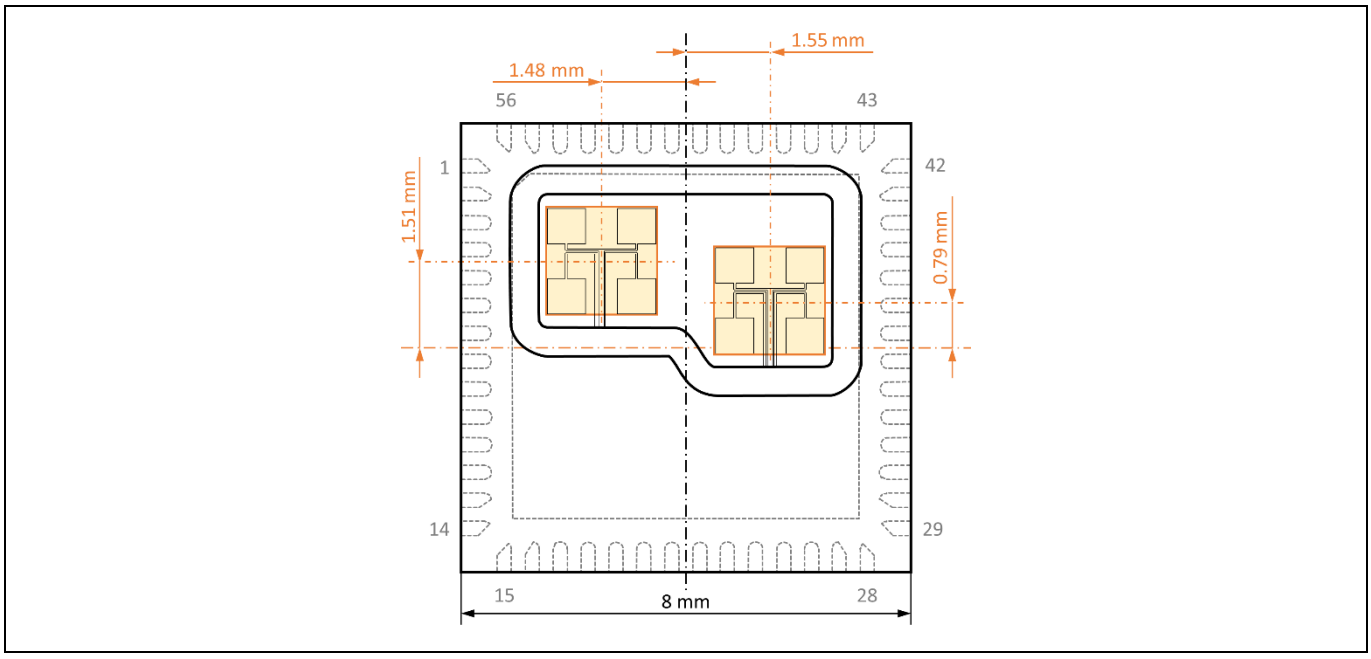


Figure 4 Antenna Position (top view)

6 Application

6.1 Application Circuit Schematic

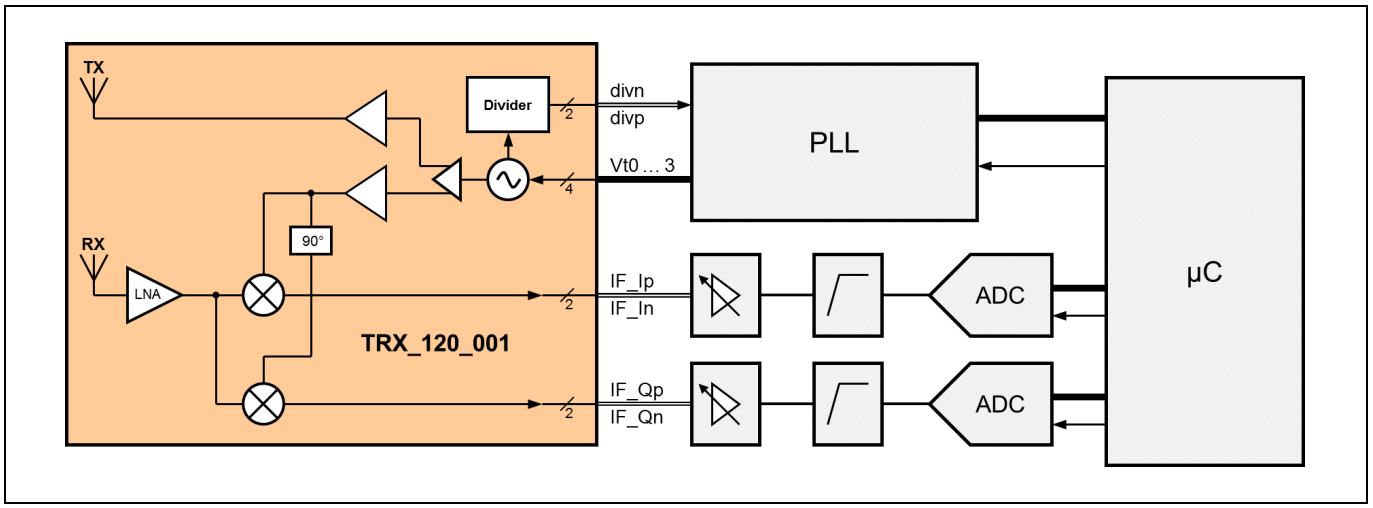


Figure 5 Application Circuit

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Boards

For a quick and easy start into radar development Silicon Radar offers SiRad Easy®. It is an evaluation board system for many of our integrated IQ transceivers with antennas in package or on PCB. It comes with a reference hardware and provides a complete design environment which can be configured via a browser-based graphical user interface. Its rich functionality and the open communication protocol make it a versatile tool – also for enhanced development projects.
It features:

- Distance measurement
- Velocity measurement
- Frequency modulated continuous wave mode (FMCW)
- Continuous wave mode (CW)

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6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

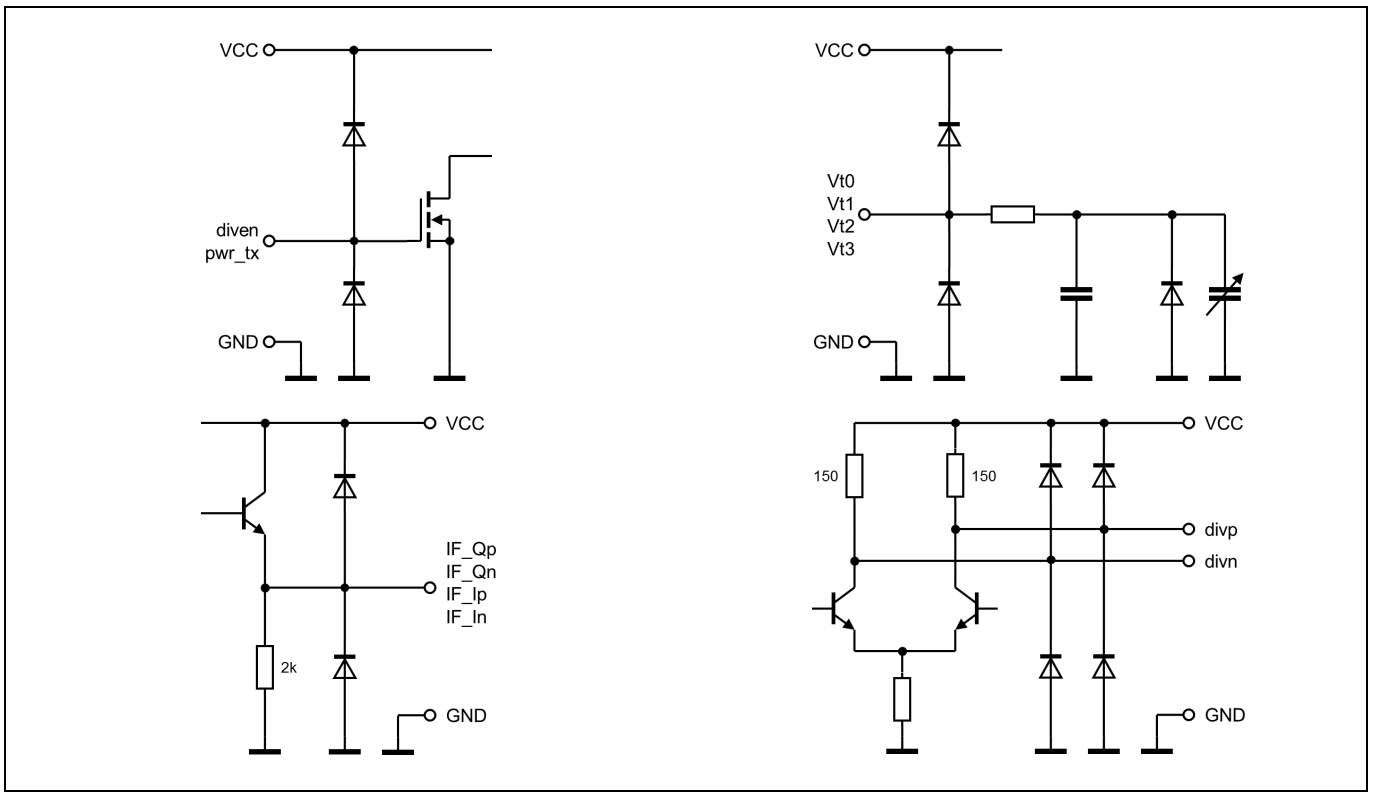

Figure 6 Equivalent I/O Circuits

6.5 VCO Tuning Inputs

The VCO tuning inputs Vt0 – Vt3 are of analog nature, but can be switched digitally as well. The tuning inputs differ in their tuning ranges (tuning bandwidth) and slopes, whereby Vt3 has the widest tuning range, and Vt0 the narrowest.

Table 6 Typical VCO Tuning Bandwidth and Slope

Input	VCO tuning bandwidth (MHz)		Middle band slope (MHz/V)	
Vt0	Δf_{TX_Vt0}	720	$\Delta f_{TX} / \Delta V_{Vt0}$	290
Vt1	Δf_{TX_Vt1}	750	$\Delta f_{TX} / \Delta V_{Vt1}$	300
Vt2	Δf_{TX_Vt2}	1580	$\Delta f_{TX} / \Delta V_{Vt2}$	630
Vt3	Δf_{TX_Vt3}	3450	$\Delta f_{TX} / \Delta V_{Vt3}$	1380

The VCO tuning range of a specific tuning input can be increased by connecting it to another tuning input. All combinations of the four tuning inputs are allowed. Unused tuning inputs must be set to a fixed potential (between 0 and V_{CC}). The interconnection of all inputs Vt0 – Vt3 leads to the maximum tuning bandwidth. For example, if Vt0 is used as tuning input, the variation of the potential at Vt1, Vt2, Vt3 in all logical combinations of 0 and V_{CC}, results in offsetting the tuning curve (see Figure 10).

7 Reliability and Environmental Test

Table 7 Reliability and Environmental Test according to JEDEC Standards

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	pass
ELFR	JESD22-A108	Running the burn-in, 48 h at 85°C in 7 runs	pass
Temperature Cycling	JESD22-A104	850 cycles at -40°C … 125°C	pass
HTSL	JESD22-A103	1,000 h at 150°C	pass
HTOL	JESD22-A108	1,000 h at 85°C	pass
THB	JESD22-A101	1,000 h at 85°C and 85% RH	pass

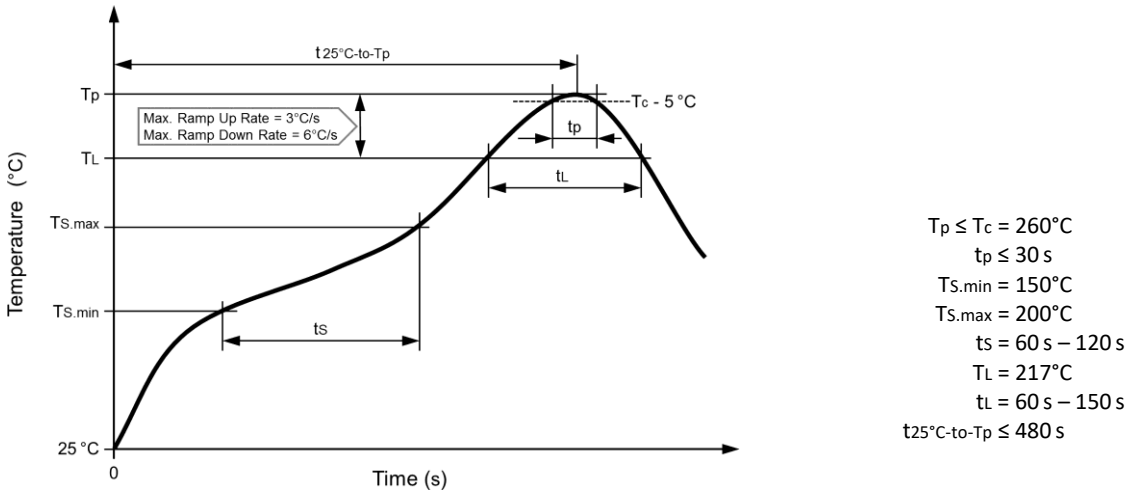

Figure 7 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

8 Measurement Results

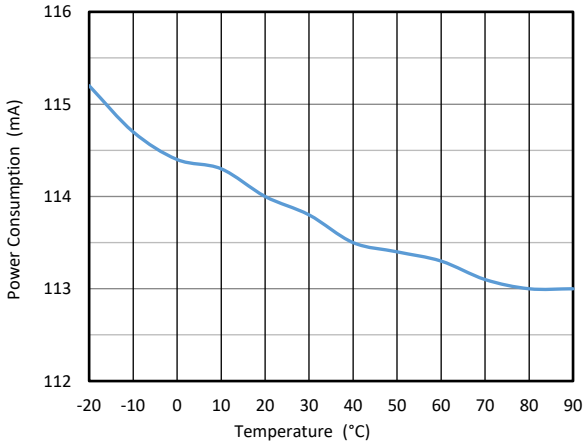

Figure 8 Power Consumption vs. Temperature

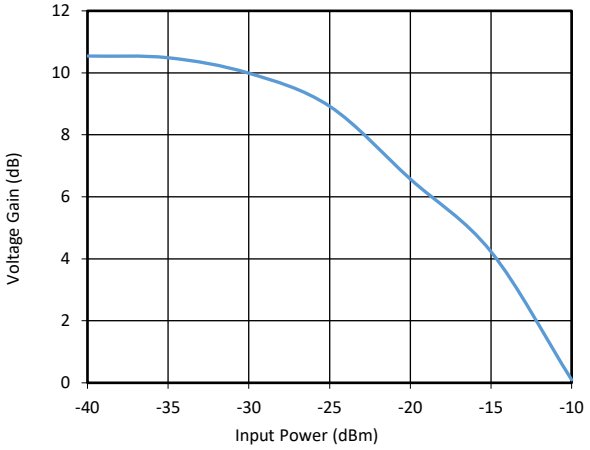

Figure 9 Measured Conversion Gain of the Receiver

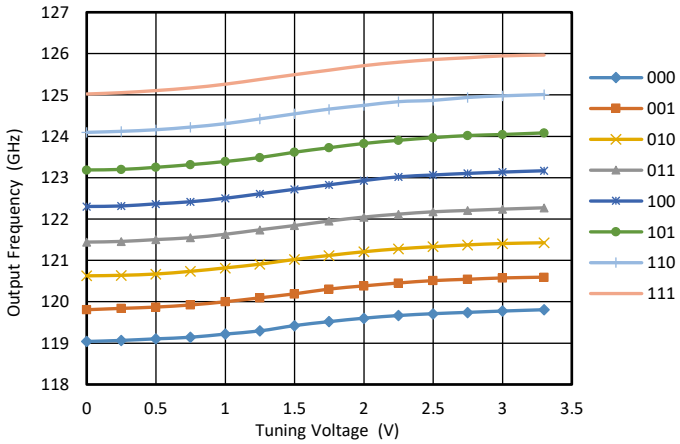

Figure 10 VCO Tuning Curves. Vt0 is varied, while Vt1, Vt2 and Vt3 are driven high or low. For example, 011 means Vt3 = 0, Vt2 = 3.3 V, and Vt1 = 3.3 V.

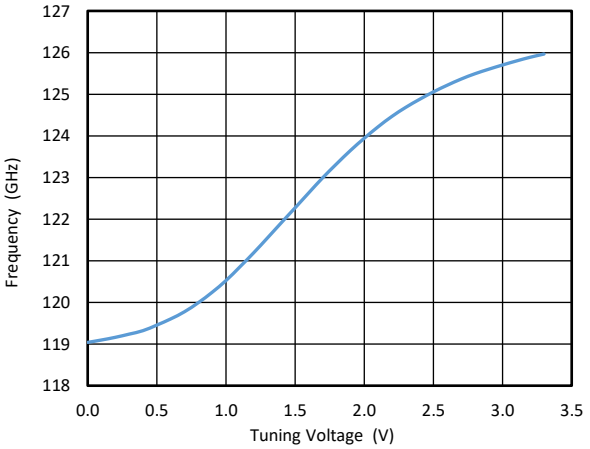

Figure 11 Full Bandwidth VCO Tuning.
Vt0, Vt1, Vt2, Vt3 are interconnected.
(Vt0 = Vt1 = Vt2 = Vt3)

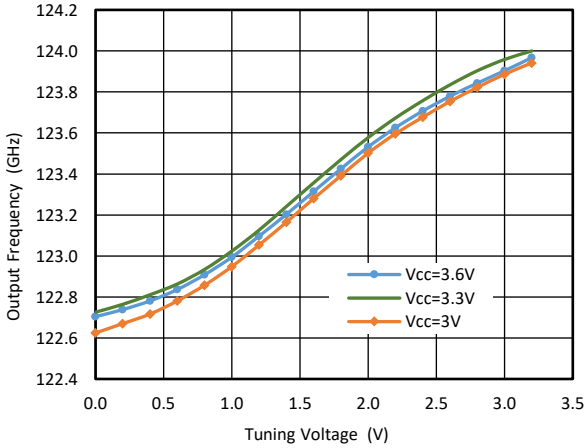

Figure 12 VCO Pushing - V_{CC} ± 300 mV
Vt0 = Sweep , Vt1 = Vt2 = 0, Vt3 = 3.3 V

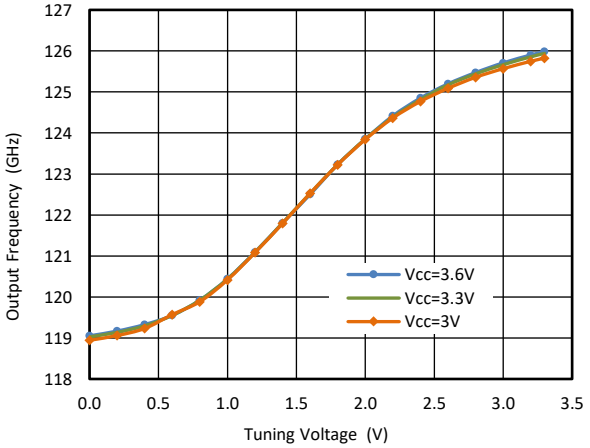

Figure 13 VCO Pushing - Full Bandwidth Operation.
All tuning voltages, Vt0 = Vt1 = Vt2 = Vt3

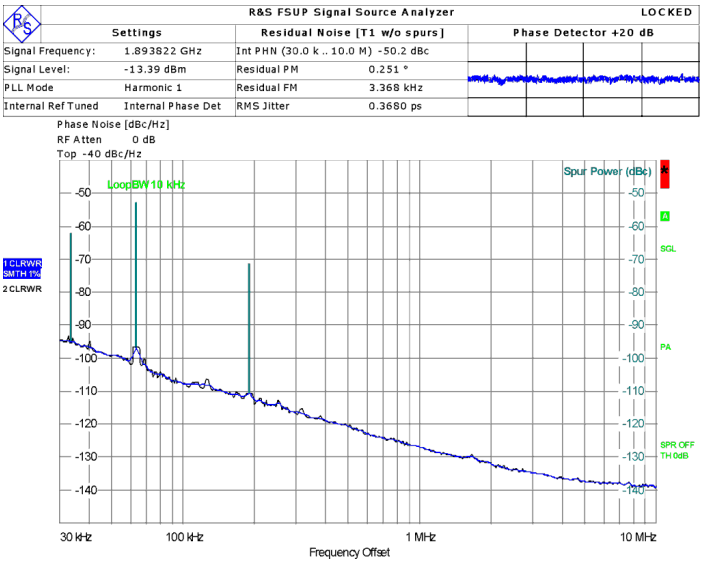

Figure 14 Phase Noise of the Integrated Oscillator Measured at Divider Output (1.89GHz)

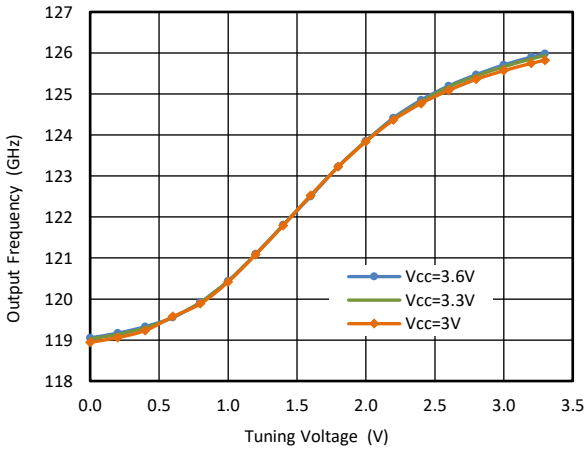

Figure 15 VCO Pushing - Full Bandwidth Operation. All tuning voltages, Vt0 = Vt1 = Vt2 = Vt3

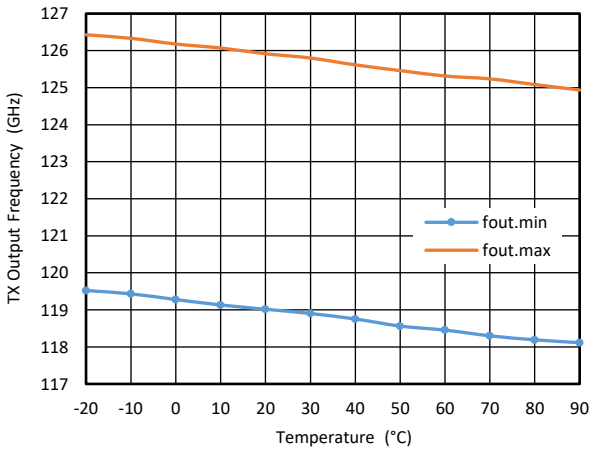

Figure 16 Output Frequency vs. Temperature

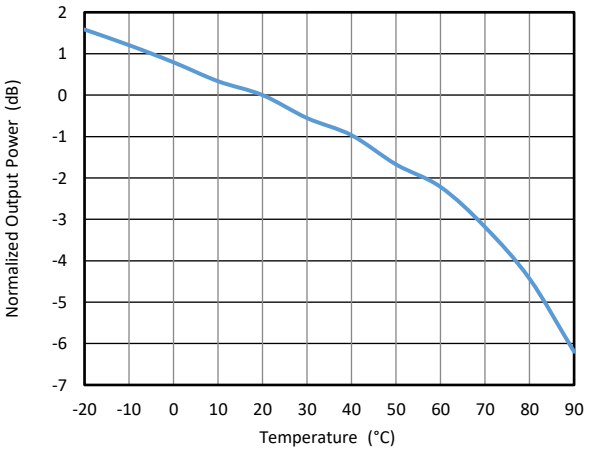

Figure 17 Output Power Swing vs. Temperature (Normalized to 20°C)

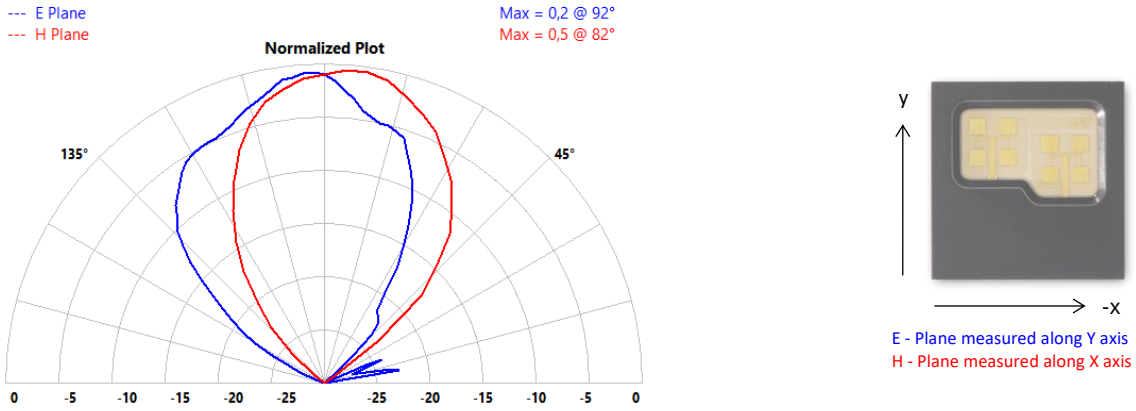

Figure 18 Combined Radiation Pattern Measurements of TX and RX Patch Antennas

Measurements above are performed by using the TRX_120_001 transceiver as an FMCW distance sensor by the help of its evaluation kit. A moving reflector around the axis is used as a target. Then, the strength of the IF signal is measured and values are normalized to 0 degrees for each axis. Therefore, the pattern does not show a pattern of single antenna, instead it gives the information of combined pattern of the TX and RX antennas in the QFN package.

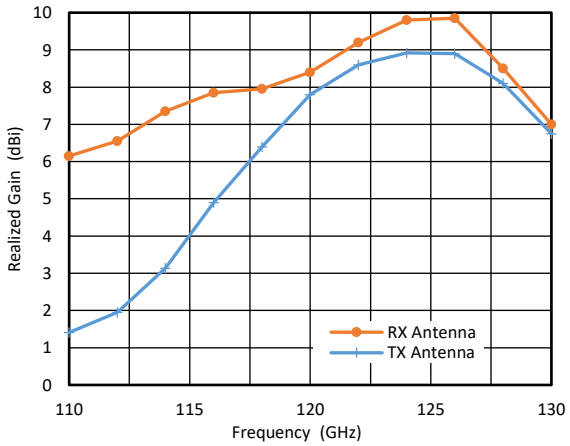

Figure 19 Simulated Single Antenna Gain vs. Frequency (Broad Side Direction)

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