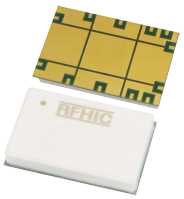
GaN Doherty Hybrid Amplifier RTH18008S-30

Product Features

- GaN on SiC Chip on Board
- Surface Mount Hybrid Type
- Asymmetric Doherty Amplifier
- High Efficiency
- No Matching circuit needed

Applications

- RF Sub-Systems
- Base Station
- RRH
- 4G/ LTE system
- Small cell



Package Type : SP-2C

Description

Accommodating the future of 4G/LTE small cells, RFHIC introduces RTH18008S-30 amplifier fabricated using an advanced high power density Gallium Nitride (GaN) semiconductor process. This high performance amplifier achieves high efficiency of 45%, and powers 8W over the frequency range from 1805MHz to 1880MHz. Integrated with Asymmetrical Doherty configurations, RTH Series is packaged in a very small form-factor 32 x 20 x 5.6mm on AIN (aluminum nitride) board which provides excellent thermal dissipation.

Electrical Specifications @ Vds =31V, Ta=25℃

PARAMETER	UNIT	MIN	TYP	MAX	CONDITION
Frequency Range	MHz	1805	-	1880	ZS = ZL = 50 ohm
Power Gain	dB	29.5	31.5	-	Drive+Carrier Idq = 270mA Vgp = -4.5V
Gain Flatness		-2	-	+2	
Input Return Loss		-6	-10	-	
Pout @ Average	dBm	-	39	-	
Pout @ Psat	dBm	46.5	-	-	Pulse Width=20us, Duty10%
ACLR @ LTE 1FA BW 20MHz(PAPR 7.5dB) C.F ± 18.015MHz	dBc	-	-29	-	Non DPD
		-	-56	-	With DPD
2nd Harmonic	dBc	-	-27	-	@Pout = 39dBm (LTE 20MHz 1FA PAPR=7.5dB)
3rd Harmonic		-	-35	-	
Drain Efficiency	%	40	45	-	Pout @ Average
Drive Idq	mA	-	50	-	
Carrier Idq		-	220	-	
Total Ids		-	570	640	
Supply Voltage	V	-	-3.0	-2.0	Vgd/Vgc
		-	-4.5	-4.0	Vgp*
		30.8	31	-	Vds

Caution

The drain voltage must be supplied to the device after the gate voltage is supplied

Turn on: Turn on the Gate voltage supply and last turn on the Drain voltage supplies

Turn off :Turn off the Drain voltage and last turn off the Gate voltage

Note

1. ACLR Measured Pout=39dBm @ fc± 20MHz / 18.015MHz
   LTE 20MHz 1FA PAPR=7.5dB @ 0.01% probability on CCDF, (DPD Engine: Xilinx DPD)
2. Vgp: Adjust Vgp lower(**Δ-1.6V)** @Peaking Amp. Idq=100mA ±5%

Mechanical Specifications

PARAMETER	UNIT	TYP	REMARK
Mass	g	7	-
Dimension	mm	32 x 20 x 5.6	-

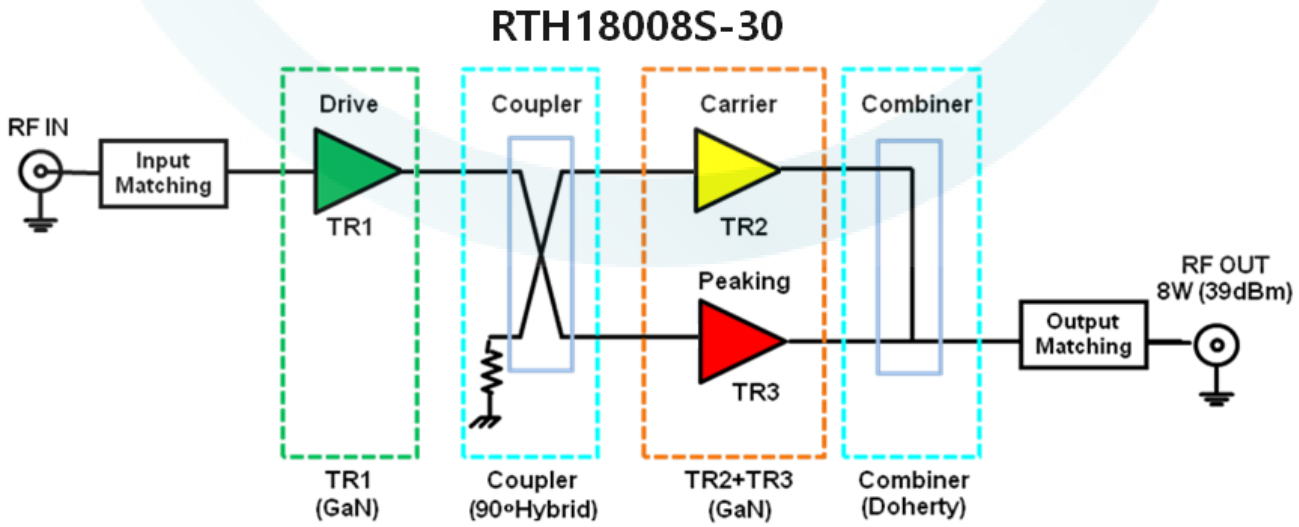
Absolute Maximum Ratings

PARAMETER	UNIT	RATING	SYMBOL
Gate-Source Voltage	V	-8 ~ -2	Vgd Vgc Vgp
Drain-Source Voltage	V	50	Vds
Gate Current	mA	12	Igs
Operating Junction Temperature	°C	225	T_J
Operating Case Temperature	°C	-30 ~ 100	T_C
Storage Temperature	°C	-40 ~ 100	T_{STG}

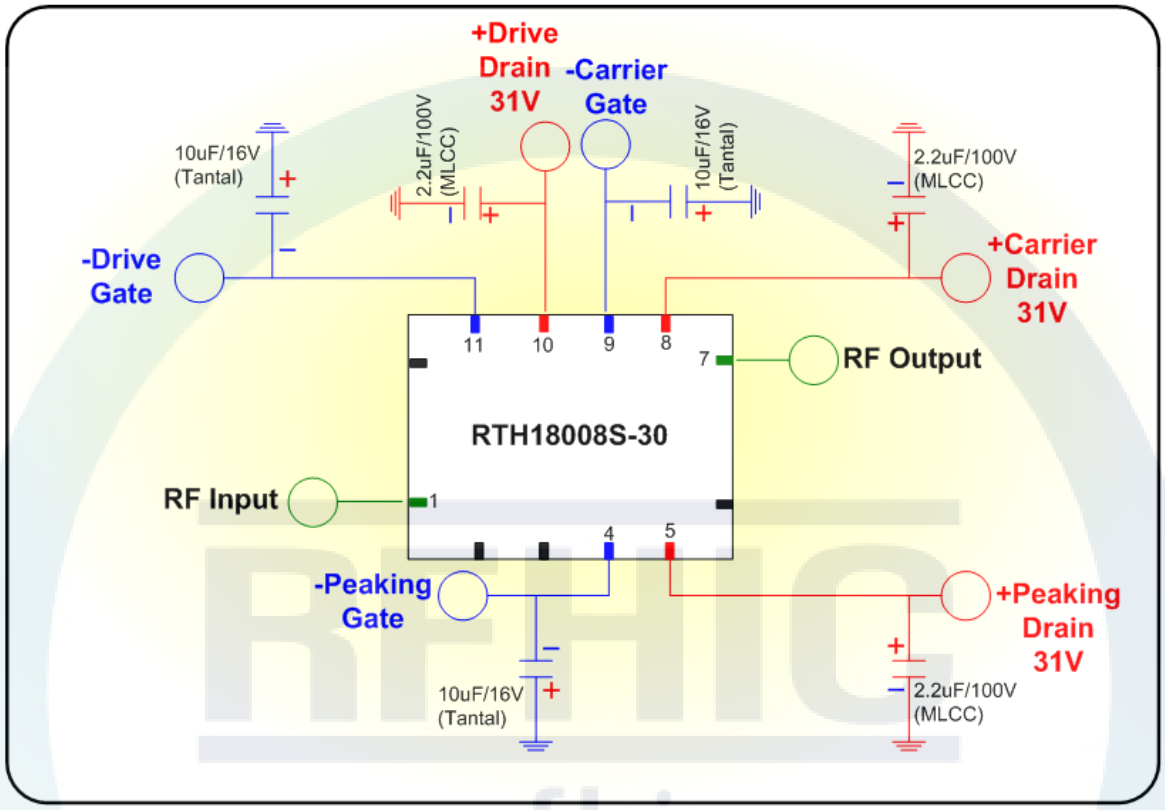
Operating Voltages

PARAMETER	UNIT	MIN	TYP	MAX	SYMBOL
Drain Voltage	V	30.8	31	-	Vds
Gate Voltage (on-stage)	V	-	Vgd @Drive Idq	-2	Vgd
Gate Voltage (on-stage)	V	-	Vgc @Carrier Idq	-2	Vgc
Gate Voltage (on-stage)	V	-	Vgp	-2	Vgp
Gate Voltage (off-stage)	V	-	-8	-	Vgd
Gate Voltage (off-stage)	V	-	-8	-	Vgc
Gate Voltage (off-stage)	V	-	-8	-	Vgp

Block Diagram



Application Circuit



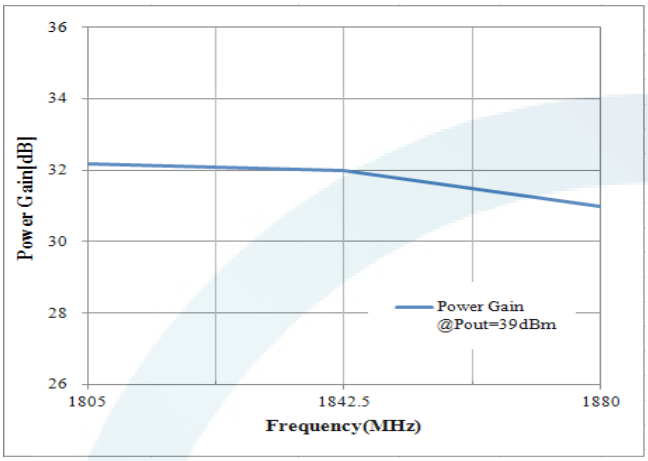
Part List

Location	Model No.	Spec.	Maker
Gate(4, 9, 11 Pin)	TAJA106K016RNJ	10uF / 16V	AVX
Drain(5, 8, 10 Pin)	GRM32ER72A225KA35_3225K	2.2uF / 100V	MURATA
Evaluation Board	RO4350B	2Layer, 30mil	ROGERS

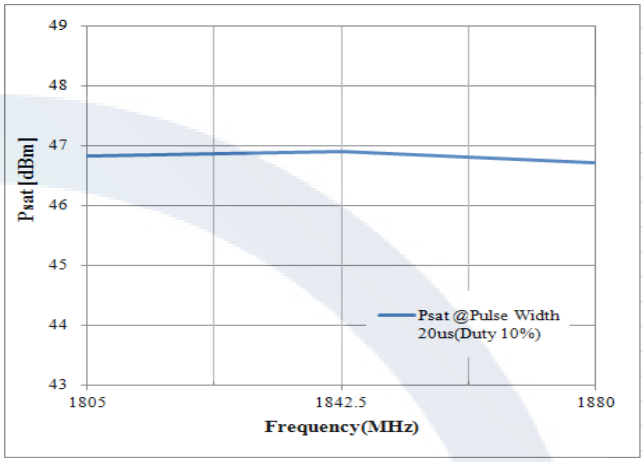
Performance Charts

* **Bias condition** @ Idq= 270mA, Vgp= -4.5V, Ta=25℃

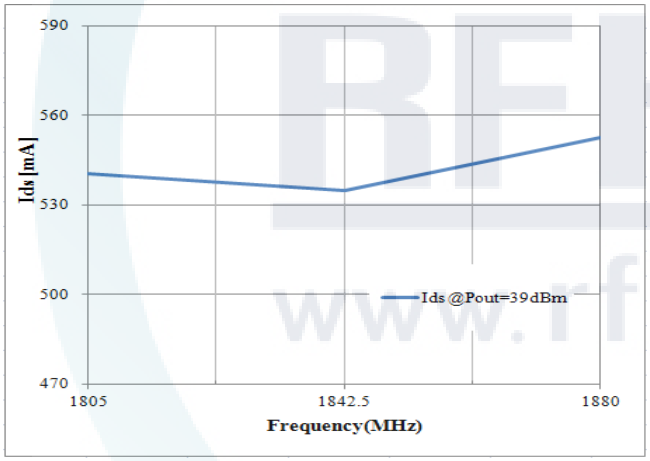
Power Gain vs. Frequency



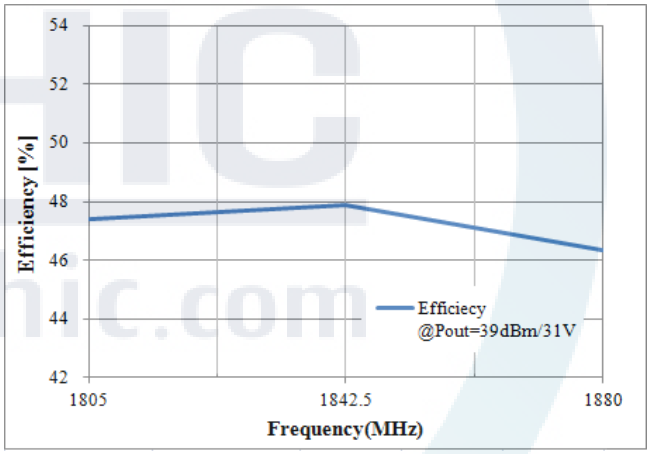
Psat vs. Frequency



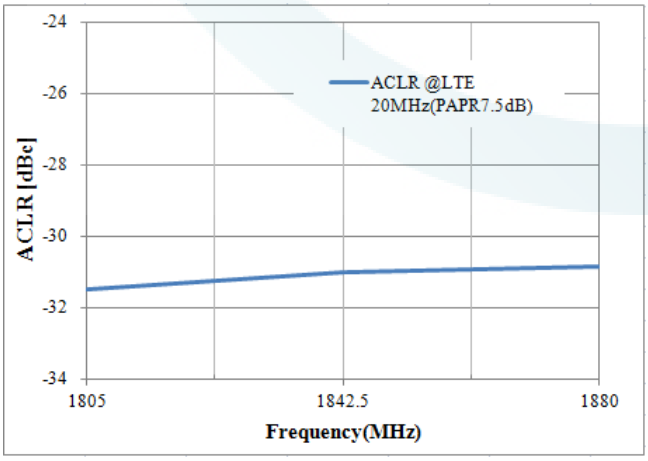
Ids vs. Frequency



Drain Efficiency vs. Frequency

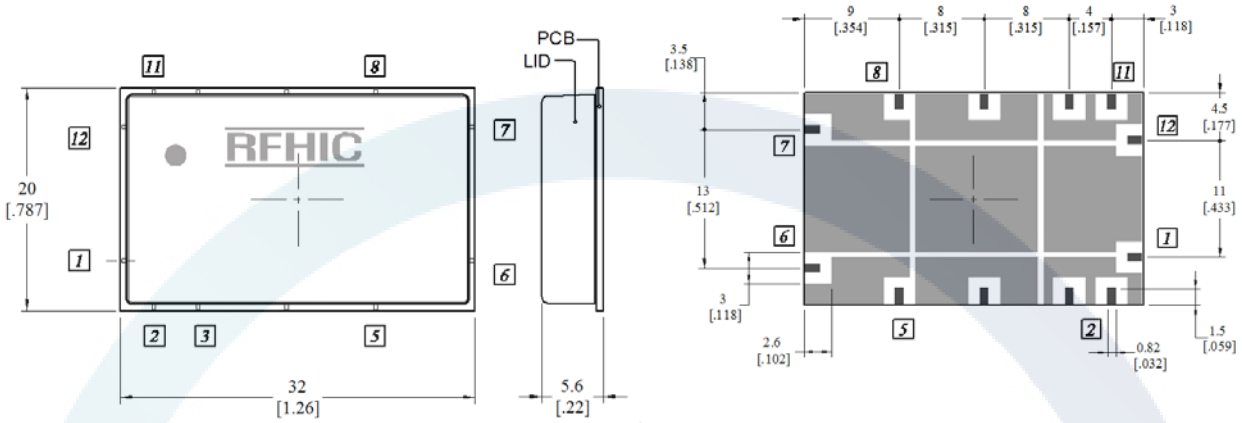


ACLR vs. Frequency



Package Dimensions (Type: SP-2C)

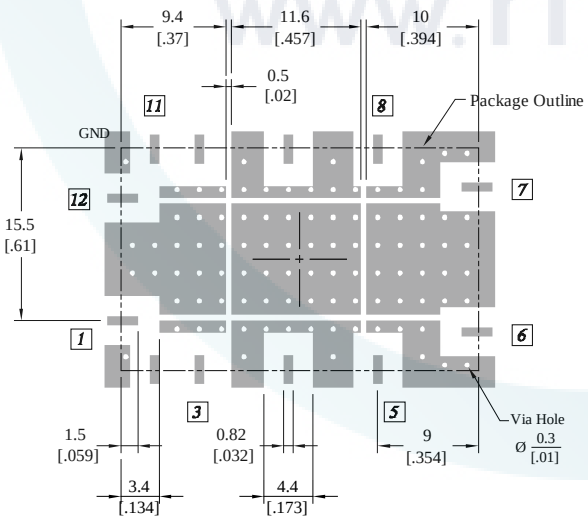
* Unit: mm[inch] | Tolerance ±0.15 [.006]



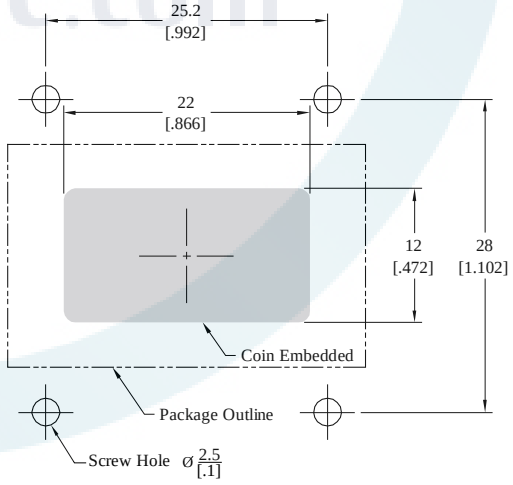
▲ Top View ▲ Side View ▲ Bottom View

Pin Description							
Pin No	**Function**	**Pin No**	**Function**	**Pin No**	**Function**	**Pin No**	**Function**
1	RF Input	4	Vgp	7	RF Output	10	Vds
2	NC/GND	5	Vds	8	Vds	11	Vgd
3	NC/GND	6	NC/GND	9	Vgc	12	NC/GND

Recommended Pattern



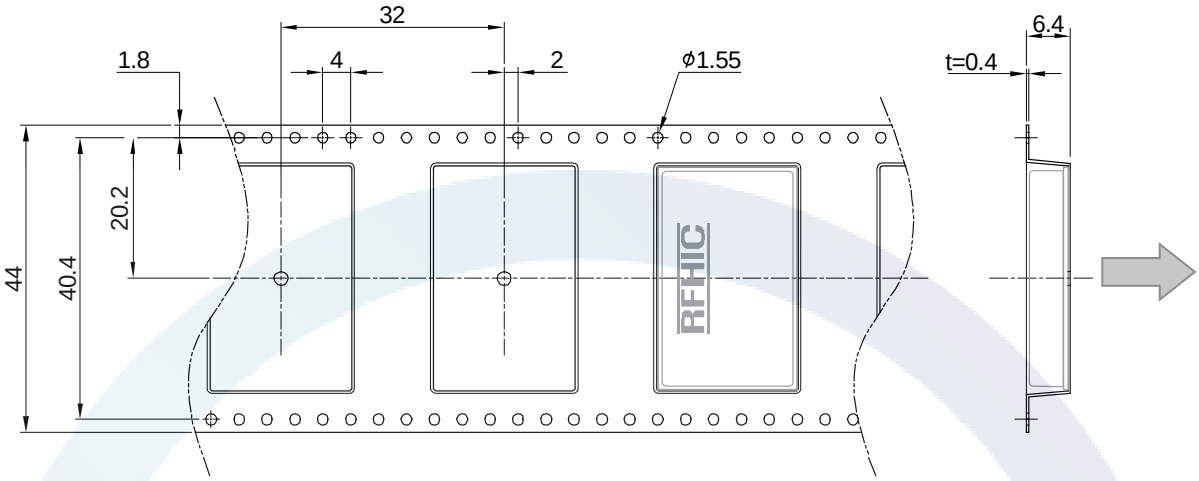
Recommended Mounting Configuration



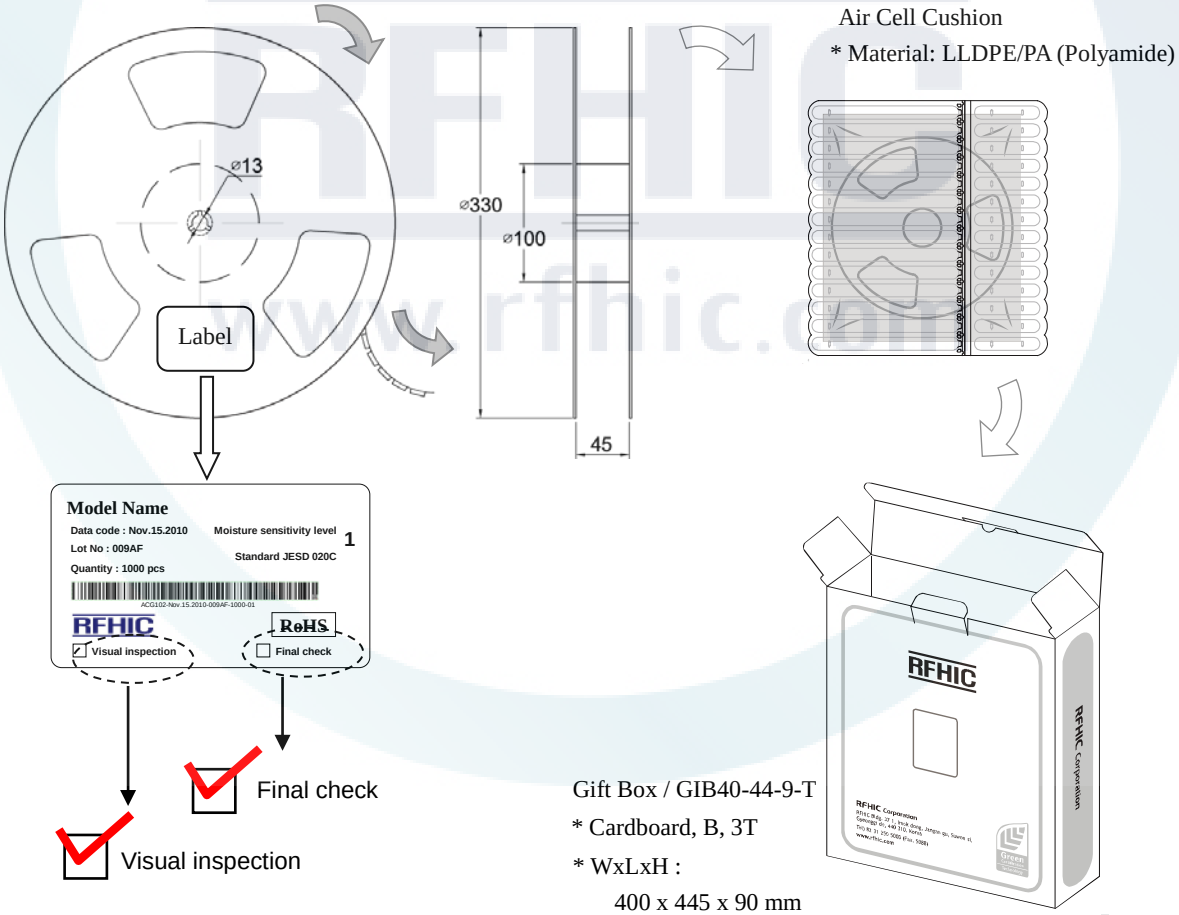
Mounting Configuration Notes

1. Ground / thermal via holes are critical for the proper performance of this device.
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via hole region contacts the heatsink.
4. Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink.
5. RF trace width depends upon the PCB material and construction.
6. Use 1 oz. Copper minimum.

Carrier Tape Dimensions in mm



Reel Dimensions in mm



Air Cell Cushion

* Material: LLDPE/PA (Polyamide)

Gift Box / GIB40-44-9-T

* Cardboard, B, 3T
* WxLxH :
  400 x 445 x 90 mm

Precautions

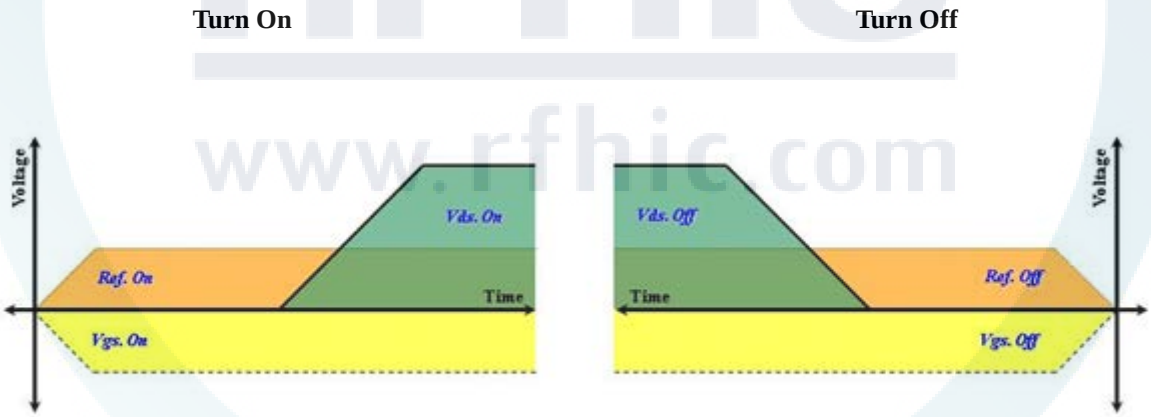
This product is a Gallium Nitride Transistor.
The Gallium Nitride Transistor requires a Negative Voltage Bias which operates alongside a Positive Voltage Bias. These Biases are applied in accordance to the Sequence during Turn-On and Turn-Off.
The Pallet Amplifier does not have a built-in Bias Sequence Circuit. Therefore, users need to either apply positive voltages and negative voltages in the required sequence, or add an external Bias Circuit to this Amplifier.
The required sequence for power supply is as follows.

During Turn-On

1. Connect GND.
2. Apply Gate Voltage (Vgd and Vgc and Vgp)
3. Apply Drain Voltage (Vds)
4. Apply the RF Power.

During Turn-Off

1. Turn off RF power.
2. Turn off Drain Voltage (Vds), and then, turn off the Gate Voltage (Vgd and Vgc and Vgp)
3. Remove all connections.



- Sequence Timing Diagram -

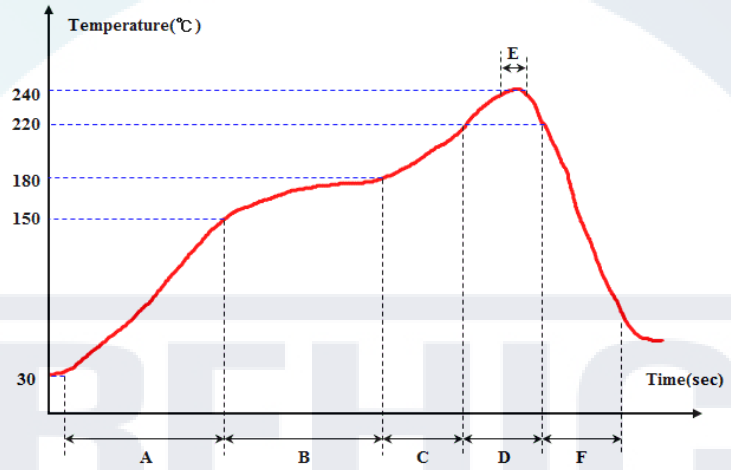
Reflow Profile

*** Reflow oven settings**

Zone	A	B	C	D	E	F
Temperature(°C)	30 ~ 150 ℃	150 ~ 180 ℃	180 ~ 220 ℃	220 ~ 220 ℃	235 ~ 240 ℃	2 ~ 6 ℃/ Sec Drop
Belt speed	55 ~ 115 sec	55 ~ 75 sec	30 ~ 50 sec	30 ~ 50 sec	5 ~ 10 sec	60 ~ 90 sec

Reflow Cycle Limit= 1time

*** Measured reflow profile**



Ordering Information

Part Number	Package Design
RTH18008S-30	-R (Reel)
	-B (Bulk)
	-EVB (Evaluation Board)

Revision History

Part Number	Release Date	Version	Modification	Data Sheet Status
RTH18008S-30	2018.09.07	2.0	Newly Created	-