BLF989E; BLF989ES

UHF power LDMOS transistor Rev. 1 — 3 April 2020

AMPLEON

Product data sheet

Product profile 1.

1.1 General description

A 1000 W LDMOS RF power transistor for asymmetrical broadcast Doherty transmitter applications which operates at 180 W DVB-T average power. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications.

Table 1. **Application information**

RF performance at $V_{DS} = 50 \text{ V}$ in an asymmetrical Doherty application.

Test signal	f	P _{L(AV)}	Gp	η _D	IMD _{shldr}	PAR
	(MHz)	(W)	(dB)	(%)	(dBc)	(dB)
DVB-T (8k OFDM) [1]	470 to 620	180	17	50	-38	8
	470 to 700	180	15	48	-37.5	7.5

^[1] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

- Designed for asymmetric Doherty operation
- Very high efficiency enabling air cooled high power transmitters
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Broadcast transmitter applications in the UHF band
- Digital broadcasting

Pinning information 2.

Table 2. **Pinning**

Pin	Description	Simplified outlin	ne Graphic symbol
BLF989E	E (SOT539A)		
1	drain1 (peak)		
2	drain2 (main)	1 2	_ 1 _
3	gate1 (peak)		5
4	gate2 (main)	3 4	5
5	source	[1]	4 —
			"
			2 sym117
BLF989E	ES (SOT539B)		
1	drain1 (peak)		
2	drain2 (main)	1 2	. 1
3	gate1 (peak)		5 -
4	gate2 (main)	3 4	3——5
5	source	[1]	4 —
			\ \int
			2 sym117
			-

^[1] Connected to flange.

Ordering information 3.

Ordering information Table 3.

Type number	Packag	² ackage					
	Name	Description	Version				
BLF989E	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A				
BLF989ES	-	earless flanged balanced ceramic package; 4 leads	SOT539B				

Limiting values

Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS(amp)main}	main amplifier drain-source voltage		-	108	V
V _{DS(amp)peak}	peak amplifier drain-source voltage		-	108	V
V _{GS(amp)main}	main amplifier gate-source voltage		-6	+11	٧
V _{GS(amp)peak}	peak amplifier gate-source voltage		-6	+11	٧
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature	[1]	-	225	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

BLF989E_BLF989ES

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	$T_{case} = 90 ^{\circ}\text{C}; V_{DS} = 50 \text{V};$ $I_{DS} = 3.5 \text{A (main)}; I_{DS} = 0 \text{A (peak)}$	0.28	K/W
		$T_{case} = 90 ^{\circ}\text{C}; V_{DS} = 50 ^{\circ}\text{V};$ $P_{L} = 180 ^{\circ}\text{W}; PAR = 8 ^{\circ}\text{dB}$	0.19	K/W

- [1] Measured under DC test conditions, with peak section off.
- [2] Measured in an ultra-wide Doherty application, using DVB-T (8k OFDM) signal, PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

6. Characteristics

Table 6. DC characteristics

 $T_i = 25$ °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Main dev	rice					
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 2.4 \text{ mA}$	108	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 240 mA	1.5	2.1	2.5	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	2.8	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	43	-	А
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V	-	-	280	nΑ
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 8.5 \text{ A}$	-	90	-	mΩ
Peak dev	rice				1	
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 3.6 \text{ mA}$	108	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 360 mA	1.5	2.0	2.5	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	2.8	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	67	-	Α
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V	-	-	280	nΑ
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 12.6 \text{ A}$	-	60	-	mΩ

Table 7. AC characteristics

 $T_i = 25$ °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Main device						
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	-	368	-	pF
Coss	output capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	-	69	-	pF
C _{rss}	reverse transfer capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	-	0.86	-	pF

Table 7. AC characteristics ... continued

 $T_i = 25$ °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
Peak dev	Peak device						
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	484	-	pF	
Coss	output capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	107	-	pF	
C _{rss}	reverse transfer capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	-	1.16	-	pF	

Table 8. RF characteristics

RF characteristics in Ampleon production test circuit, $T_{case} = 25$ °C; unless otherwise specified.

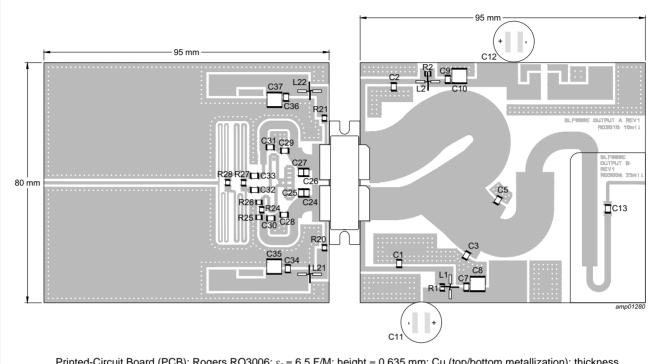
Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
DVB-T (8	DVB-T (8k OFDM), Doherty operation						
V _{DS}	drain-source voltage		-	50	-	V	
I_{Dq}	quiescent drain current	peak section: $V_{GS} = 1.3 \text{ V}$ below $V_{GS(th)}$ (peak)	-	600	-	mA	
$P_{L(AV)}$	average output power	f = 550 MHz	-	180	-	W	
Gp	power gain	f = 550 MHz	18.6	20	-	dB	
η_{D}	drain efficiency	f = 550 MHz	50	52	-	%	
PAR	peak-to-average ratio	f = 550 MHz	6.9	7.4	-	dB	

7. Test information

7.1 Ruggedness in Doherty operation

The BLF989E and BLF989ES are capable of withstanding a load mismatch corresponding to VSWR 10 : 1 through all phases under the following conditions: $V_{DS} = 50 \text{ V}$; f = 550 MHz at rated load power.

7.2 Test circuit



Printed-Circuit Board (PCB): Rogers RO3006; $\varepsilon_r = 6.5$ F/M; height = 0.635 mm; Cu (top/bottom metallization); thickness copper plating = 29.6 μ m; Rogers RO3010; ϵ_r = 10 F/M; height = 0.254 mm.

See Table 9 for a list of components.

Fig 1. Component layout for production RF test circuit

Table 9. List of components See Figure 1 for component layout.

Component	Description	Value	Remarks
C1, C2, C7, C9, C13	multilayer ceramic chip capacitor	100 pF [1]	ATC 800B
C3	multilayer ceramic chip capacitor	10 pF [1]	ATC 800B
C5	multilayer ceramic chip capacitor	8.2 pF [1]	ATC 800B
C8, C10	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK
C11, C12	electrolytic capacitor	470 μF, 63 V	
L1, L2	one turn inductor	D = 5 mm, d = 1mm	
R1	chip resistor	1 Ω	SMD 1206
R2	chip resistor	5.6 Ω	SMD 1206
C24, C25, C26, C27	multilayer ceramic chip capacitor	20 pF [1]	ATC 800B
C28, C29	multilayer ceramic chip capacitor	10 pF [1]	ATC 800B
C30, C31	multilayer ceramic chip capacitor	5.1 pF [1]	ATC 800B
C32, C33, C34, C36	multilayer ceramic chip capacitor	100 pF [1]	ATC 800B
C35, C37	multilayer ceramic chip capacitor	4.7 μF, 63 V	TDK
L21, L22	one turn inductor	D = 5 mm, d = 1mm	
R20, R21	chip resistor	5.6 Ω	SMD 0805
R25, R26	chip resistor	300 Ω	SMD 1206

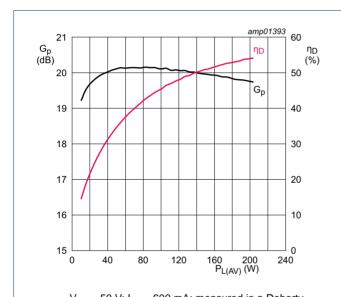
Table 9. List of components ...continued See Figure 1 for component layout.

Component	Description	Value	Remarks
R24	chip resistor	18 Ω	SMD 1206
R27	chip resistor	2x510 Ω	SMD 1206
R28	chip resistor	2x180 Ω	SMD 1206

[1] American Technical Ceramics type 800B or capacitor of same quality.

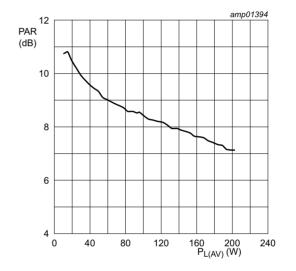
7.3 Graphs

7.3.1 DVB-T in production test circuit



 V_{DS} = 50 V; I_{Dq} = 600 mA; measured in a Doherty production test circuit at 550 MHz.

Fig 2. Power gain and drain efficiency as function of average output power; typical values



 V_{DS} = 50 V; I_{Dq} = 600 mA; measured in a Doherty production test circuit at 550 MHz.

Fig 3. Peak-to-average power ratio as a function of average output power; typical values

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8. Package outline

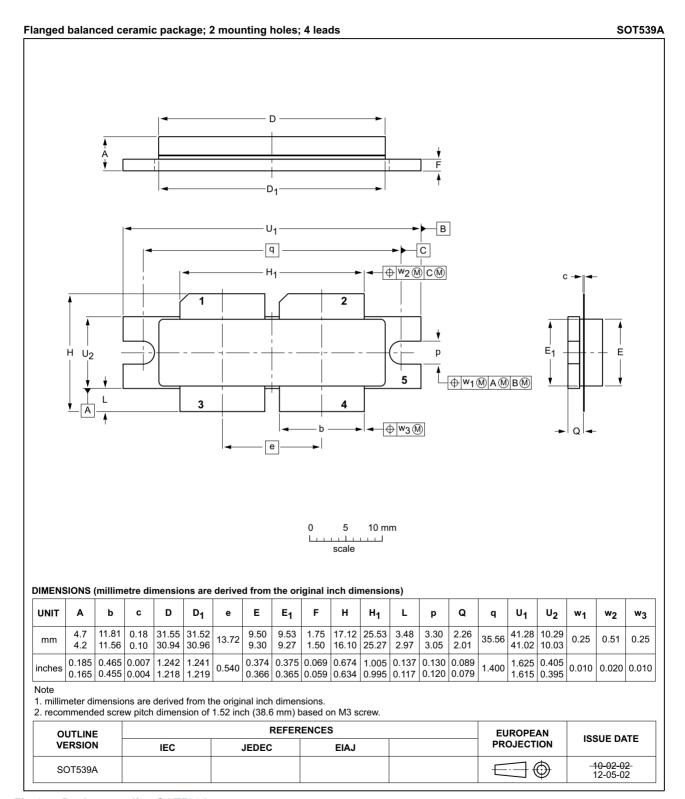


Fig 4. Package outline SOT539A

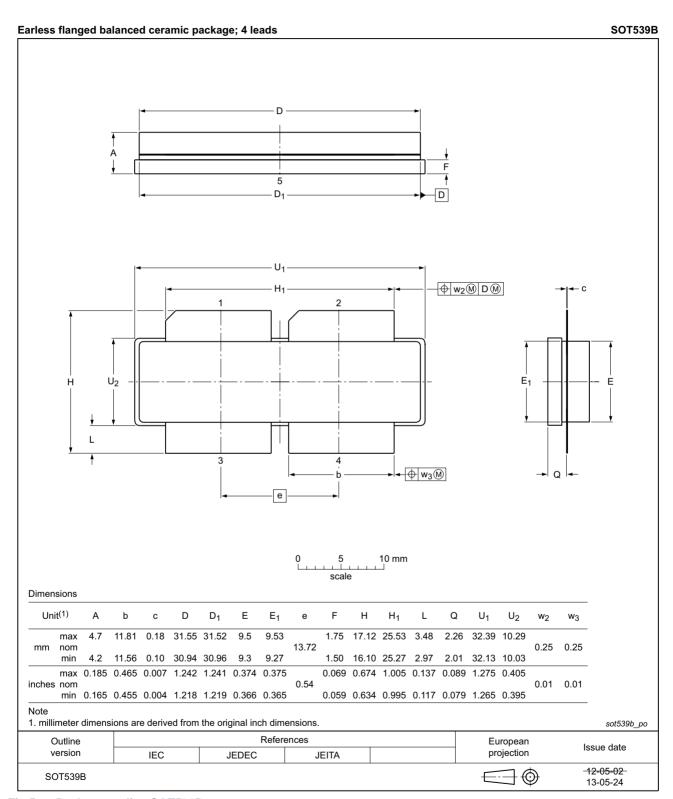


Fig 5. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

- [1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.
- [2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description	
CCDF	Complementary Cumulative Distribution Function	
DVB-T	Digital Video Broadcast - Terrestrial	
ESD	ElectroStatic Discharge	
LDMOS	Laterally Diffused Metal-Oxide Semiconductor	
MTF	Median Time to Failure	
OFDM	Orthogonal Frequency Division Multiplexing	
PAR	Peak-to-Average Ratio	
RoHS	Restriction of Hazardous Substances	
SMD	Surface Mounted Device	
UHF	Ultra High Frequency	
VSWR	Voltage Standing Wave Ratio	

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF989E_BLF989ES v.1	20200403	Product data sheet	-	-

12. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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UHF power LDMOS transistor

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