BLF978P

HF / VHF power LDMOS transistor

AMPLEON

Rev. 1 — 3 April 2020

Product data sheet

1. Product profile

1.1 General description

A 1200 W LDMOS power transistor for broadcast applications and industrial applications in the HF to 700 MHz band.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW pulsed [1]	225	50	1200	25.5	80.0
CW pulsed [2]	352	50	1150	25.0	79.6
CW [2]	352	50	1150	23.6	76.7
CW [3]	500	45	800	22.3	71.6
CW [4]	650	50	1000	20.0	66.2

[1] On production test circuit t_p = 100 μs; δ = 10 %.

[2] AR191160.

[3] AR191195.

[4] AR201049.

1.2 Features and benefits

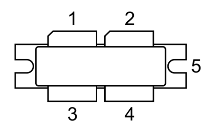
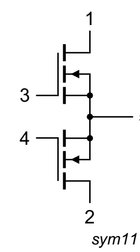
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (10 MHz to 700 MHz)
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF978P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	108	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

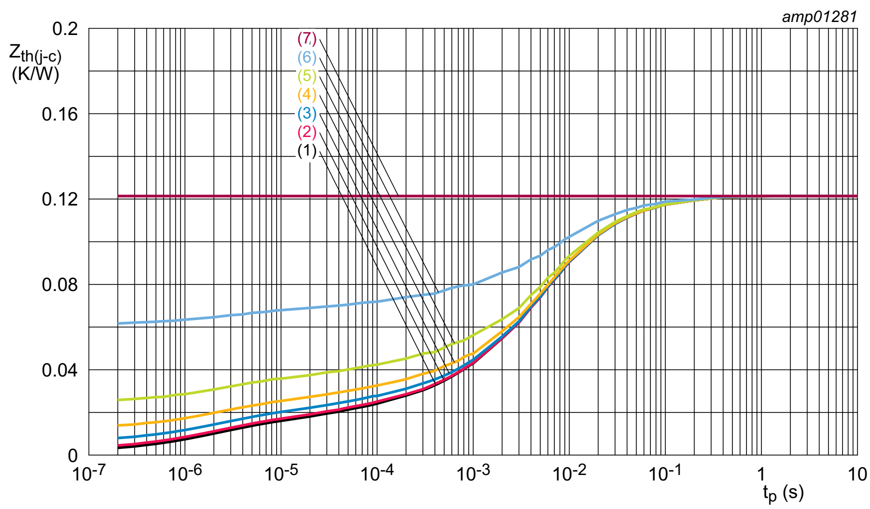
5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C [1]	0.121	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_{case} = 90 °C; t_p = 100 μs; δ = 10 % [2]	0.033	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

[2] See Figure 1.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

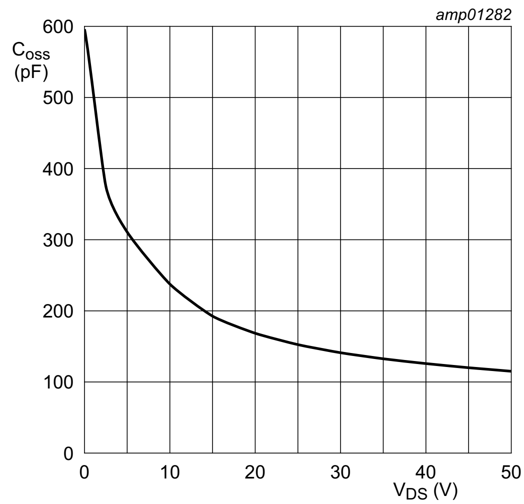
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.94 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 394 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	54	71.7	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 13.79 A	-	54	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	1.45	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	392	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	115	-	pF



V_{GS} = 0 V; f = 1 MHz.

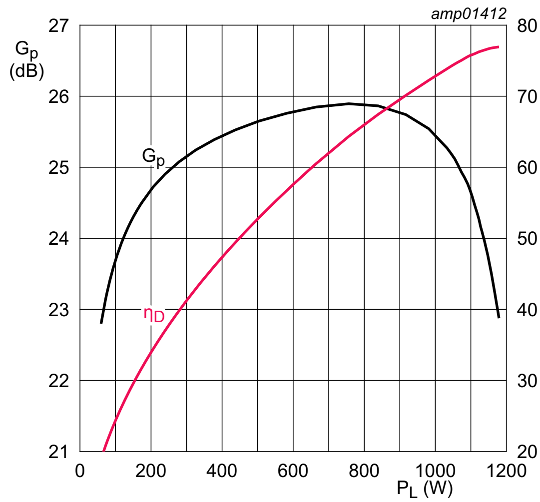
Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

Table 8. RF characteristics

Test signal: CW pulsed; t_p = 100 μs; δ = 10 %; f = 225 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 50 mA per section; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

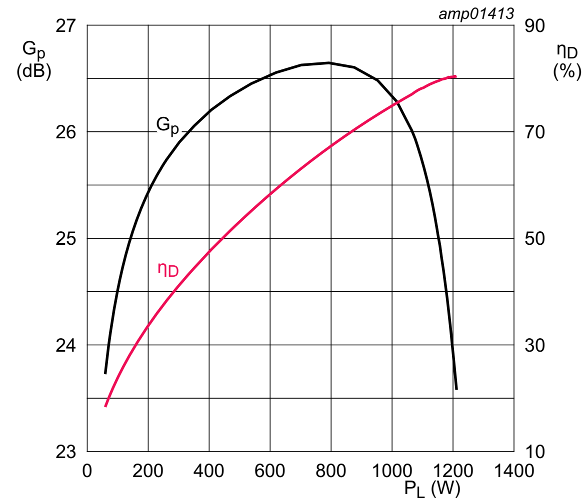
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 1200 W	23	24.5	-	dB
RL_{in}	input return loss	P_L = 1200 W	-	–20	–12	dB
η_D	drain efficiency	P_L = 1200 W	78	80.6	-	%

7. Application information



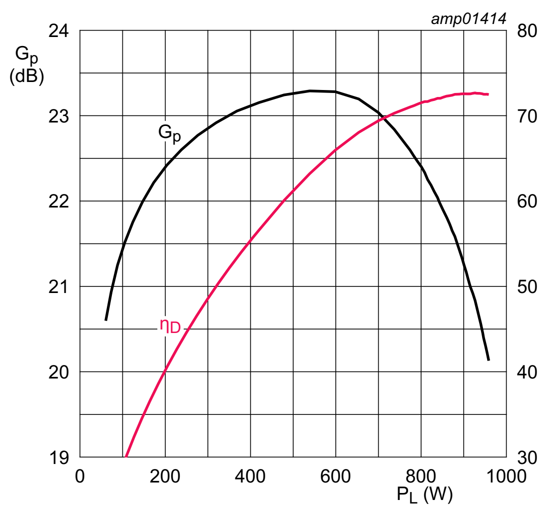
V_{DS} = 50 V; I_{Dq} = 2 × 5 mA; f = 352 MHz; CW.

Fig 3. Power gain and drain efficiency on AR191160 as function of output power; typical values



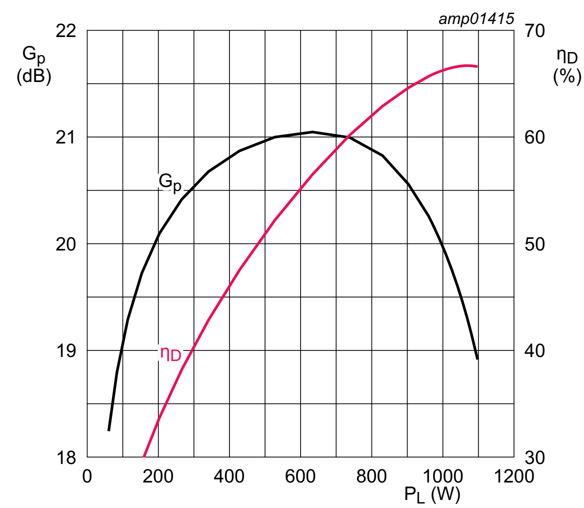
V_{DS} = 50 V; I_{Dq} = 2 × 50 mA; f = 352 MHz; CW pulsed (t_p = 100 μs; δ = 10 %).

Fig 4. Power gain and drain efficiency on AR191160 as function of output power; typical values



V_{DS} = 45 V; I_{Dq} = 2 × 10 mA; f = 500 MHz; CW.

Fig 5. Power gain and drain efficiency on AR191195 as function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 2 × 10 mA; f = 650 MHz; CW.

Fig 6. Power gain and drain efficiency on AR201049 as function of output power; typical values

8. Test information

8.1 Ruggedness in class-AB operation

The BLF978P is capable of withstanding a load mismatch corresponding to VSWR = 13 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 50 mA per section; P_L = 1200 W; f = 225 MHz; CW pulsed (t_p = 100 μs; δ = 10 %).

8.2 Impedance information

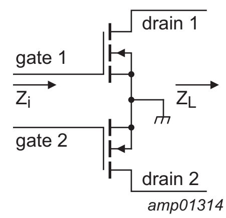


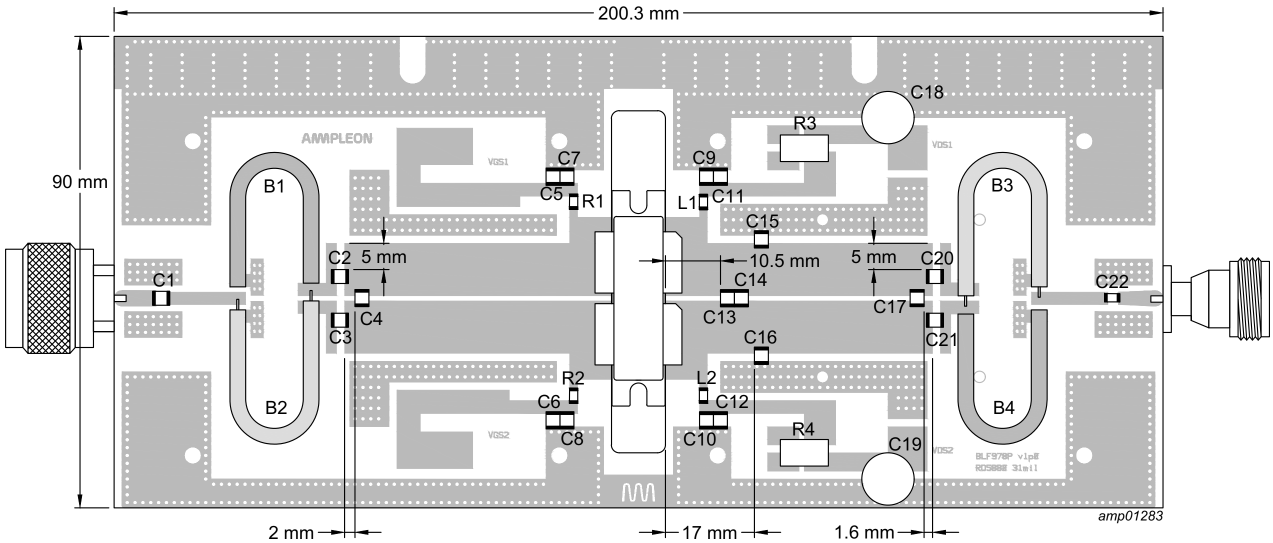
Fig 7. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 1200 W.

f	Z_i	Z_L
(MHz)	**(Ω)**	**(Ω)**
225	1.1 – j4.4	3.7 + j1.1

8.3 Test circuit



Printed-Circuit Board (PCB): Rogers RT/duroid 5880; thickness = 0.79 mm.

See Table 10 for a list of components.

Fig 8. Component layout for class-AB production test circuit

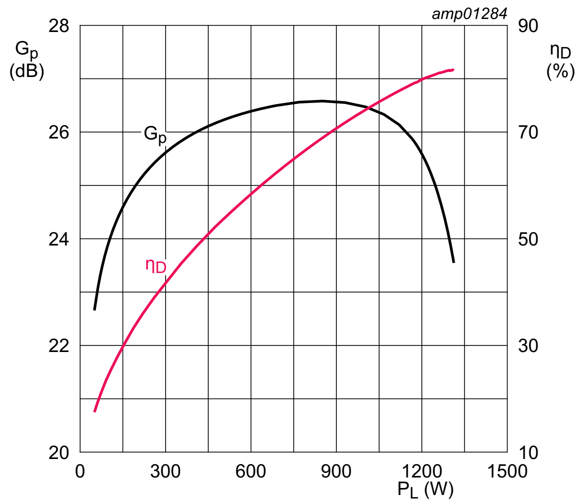
Table 10. List of components

For test circuit see Figure 8.

Component	Description	Value	Remarks
C1, C7, C8, C9, C10, C22	multilayer ceramic chip capacitor	1 nF	ATC 100B
C2, C3	multilayer ceramic chip capacitor	62 pF	ATC 100B
C4	multilayer ceramic chip capacitor	111 pF	ATC 100B
C5, C6, C11, C12	multilayer ceramic chip capacitor	4.7 μF, 100 V	C3225X7S2A475K200AE
C13, C14, C20, C21	multilayer ceramic chip capacitor	47 pF	ATC 100B
C15, C16	multilayer ceramic chip capacitor	43 pF	ATC 100B
C17	multilayer ceramic chip capacitor	51 pF	ATC 100B
C18, C19	electrolytic capacitor	1500 μF, 80 V	
L1, L2	air core inductor	17.5 nH	B06TJLB
R1, R2	SMD resistor	5.1 Ω	SMD 1206
R3, R4	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER
B1, B2, B3, B4	coaxial line	50 Ω, 58 mm	HUBER+SUHNER: EZ-141-AL-TP-M17

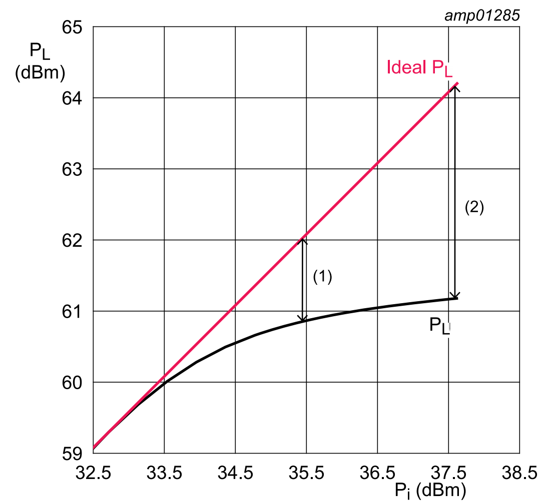
8.4 Graphical data

8.4.1 1-Tone CW pulsed



V_{DS} = 50 V; I_{Dq} = 2 × 50 mA; f = 225 MHz; t_p = 100 μs; δ = 10 %.

Fig 9. Power gain and drain efficiency as function of output power; typical values

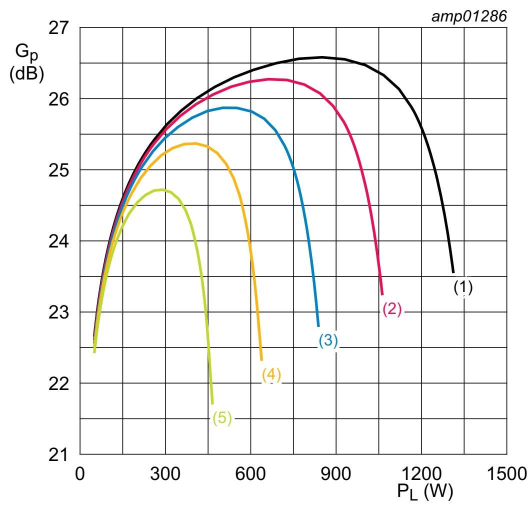


V_{DS} = 50 V; I_{Dq} = 2 × 50 mA; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) $P_{L(1dB)}$ = 60.79 dBm (1200 W)

(2) $P_{L(3dB)}$ = 61.17 dBm (1310 W)

Fig 10. Output power as a function of input power; typical values



I_{Dq} = 2 × 50 mA; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 50 V

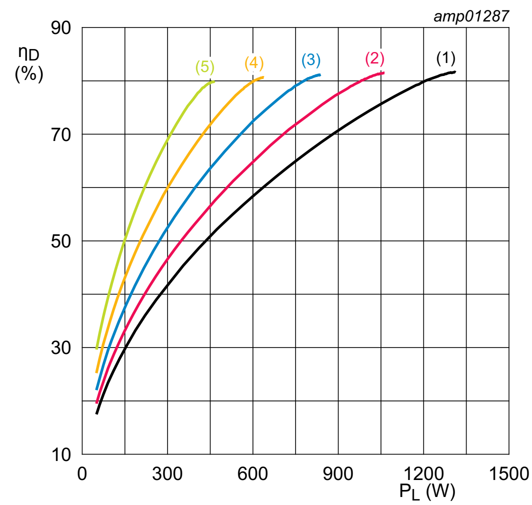
(2) V_{DS} = 45 V

(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

Fig 11. Power gain as a function of output power; typical values



I_{Dq} = 2 × 50 mA; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 50 V

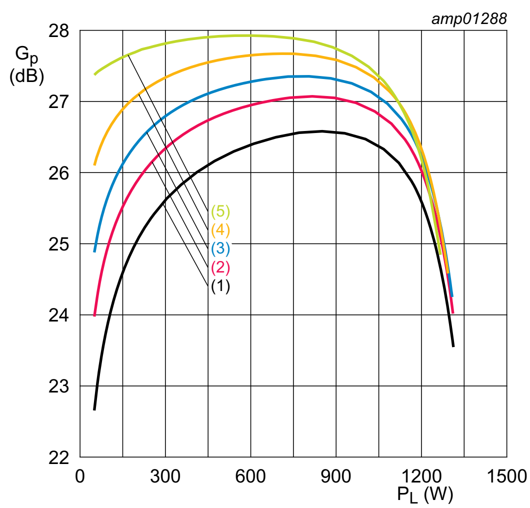
(2) V_{DS} = 45 V

(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

Fig 12. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 2 × 50 mA

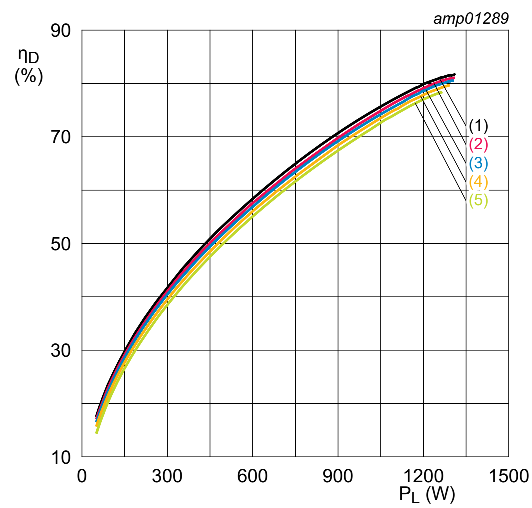
(2) I_{Dq} = 2 × 200 mA

(3) I_{Dq} = 2 × 400 mA

(4) I_{Dq} = 2 × 800 mA

(5) I_{Dq} = 2 × 1400 mA

Fig 13. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 225 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 2 × 50 mA

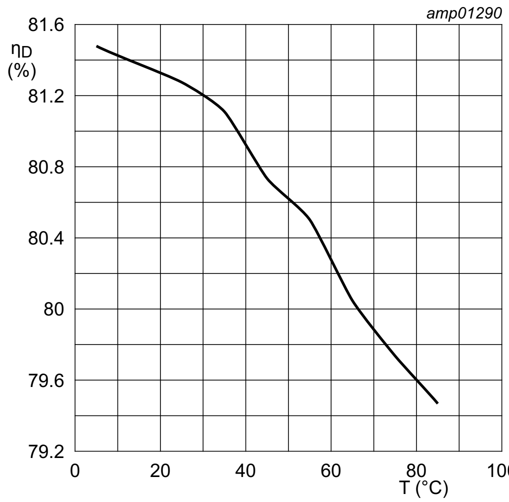
(2) I_{Dq} = 2 × 200 mA

(3) I_{Dq} = 2 × 400 mA

(4) I_{Dq} = 2 × 800 mA

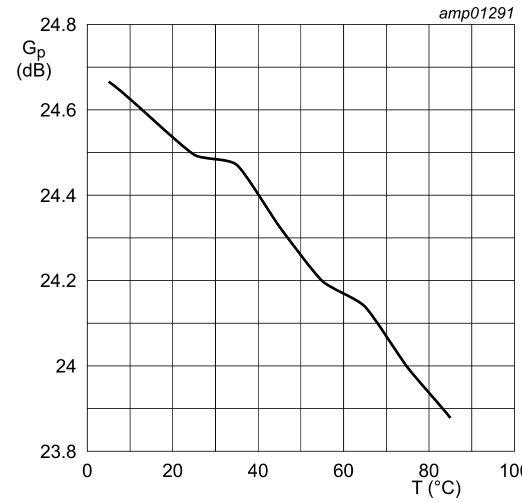
(5) I_{Dq} = 2 × 1400 mA

Fig 14. Drain efficiency as a function of output power; typical values



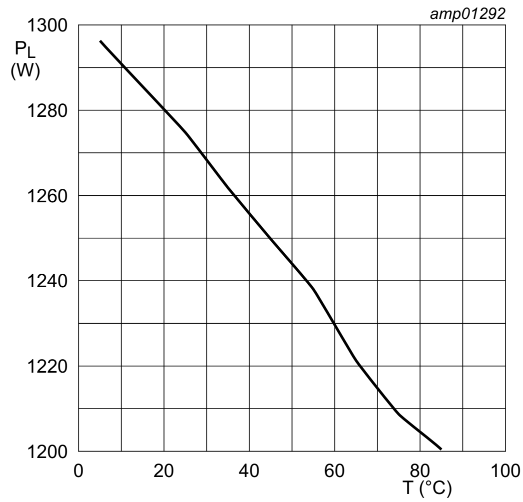
V_{DS} = 50 V; I_{Dq} = 2 × 50 mA; f = 225 MHz; at $P_{L(2dB)}$.

Fig 15. Drain efficiency as a function of temperature; typical values



V_{DS} = 50 V; I_{Dq} = 2 × 50 mA; f = 225 MHz; at $P_{L(2dB)}$.

Fig 16. Power gain as a function of temperature; typical values

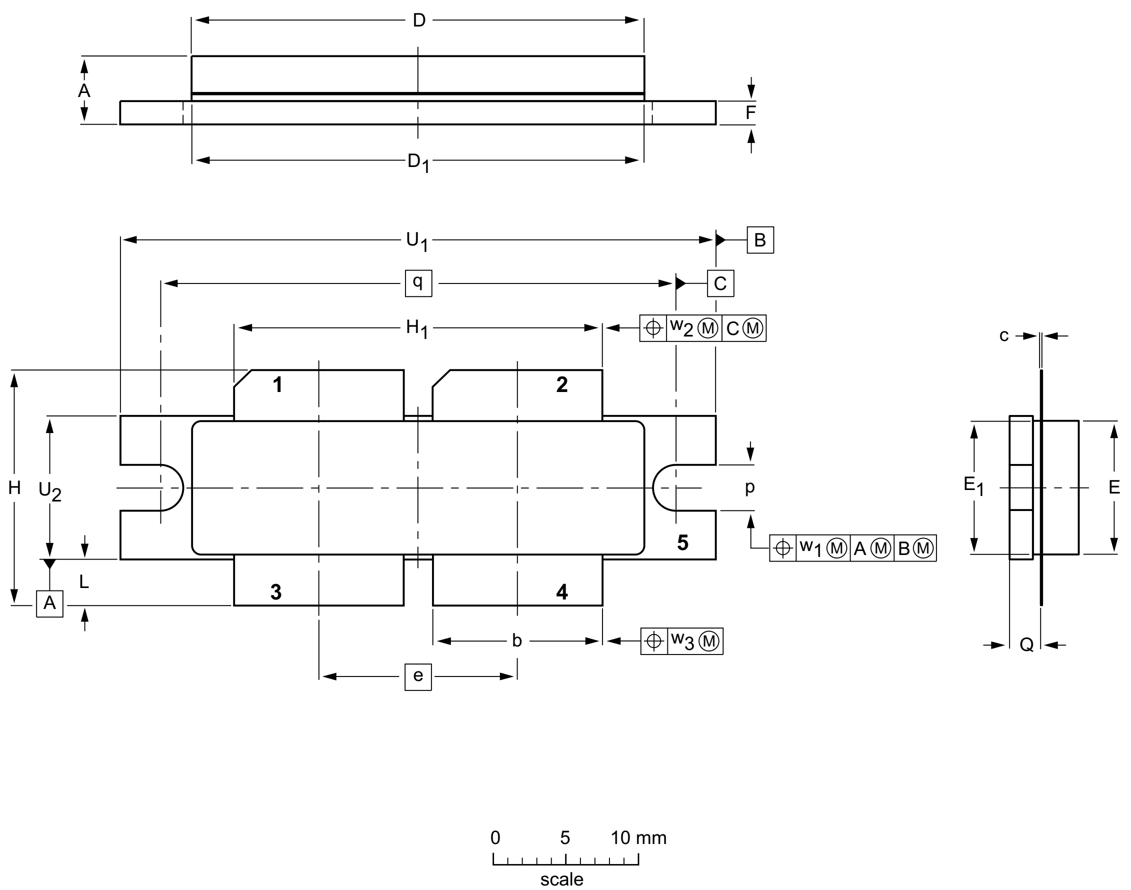


V_{DS} = 50 V; I_{Dq} = 2 × 50 mA; f = 225 MHz; at $P_{L(2dB)}$.

Fig 17. Output power as a function of temperature; typical values

9. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 18. Package outline SOT539A

10. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF978P v.1	20200403	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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15. Contents

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