

0708N (.065" x .080")

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◆ Product Features

High Q, Low ESR EIA size capacitors for RF Power Applications

◆ Product Application

Typical Applications: WiMAX/LTE (Long Term Evolution), UHF/RF High-Power Amplifiers, HDTV Transmitters, Microwave Heating Industrial/Commercial

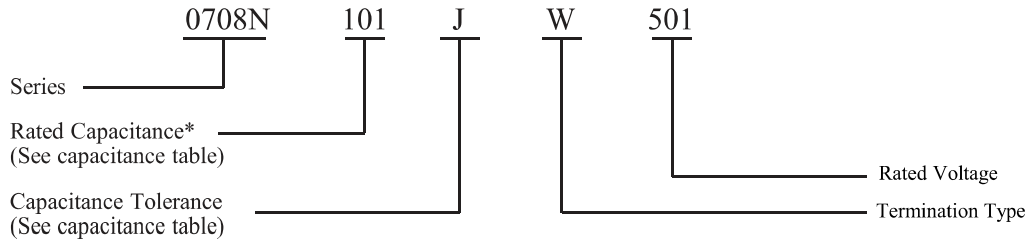
Typical Circuit Applications: Bypass, DC Blocking, Output Coupling, Antenna Coupling, Matching Networks, High RF Power Filter Networks

◆ 0708N Capacitance & Rated Voltage Table

Cap. pF	Code	Tol.	Rated WVDC	Cap. pF	Code	Tol.	Rated WVDC	Cap. pF	Code	Tol.	Rated WVDC
1.0	1R0	B,C	500V Code 501	3.9	3R9	B,C	500V Code 501	22	220	G,J	500V Code 501
1.1	1R1			4.3	4R3			24	240		
1.2	1R2			4.7	4R7			27	270		
1.3	1R3			5.1	5R1			30	300		
1.4	1R4			5.6	5R6			33	330		
1.5	1R5			6.2	6R2			36	360		
1.6	1R6			6.8	6R8			39	390		
1.7	1R7			7.5	7R5			43	430		
1.8	1R8			8.2	8R2			47	470		
1.9	1R9			9.1	9R1			51	510		
2.0	2R0			10	100	G,J		56	560		
2.1	2R1			11	110			62	620		
2.2	2R2			12	120			68	680		
2.4	2R4			13	130			75	750		
2.7	2R7			15	150			82	820		
3.0	3R0			16	160			91	910		
3.3	3R3			18	180			100	101		
3.6	3R6			20	200						

Remark: special capacitance, tolerance and WVDC are available, consult with PASSIVE PLUS.

◆ Part Numbering



*When capacitance is less than 10pF, use "R" for decimal

Capacitance Tolerance				
Code	B	C	G	J
Tol.	±0.1pF	±0.25pF	±2%	±5%

◆ 0708N Chip Dimensions

unit:inch(millimeter)

Series	Term. Code	Type/Outlines	Capacitor Dimensions				Plated Material
			Length Lc	Width Wc	Thickness Tc	Overlap B	
0708N	W		.065 ± 0.006 (1.65 ± 0.15)	.080 ± .006 (2.02 ± 0.15)	.100 ± .008 (2.54 ± 0.2)	0.020 ± .004 (0.50 ± 0.1)	100% Sn (RoHS)
	L						Tin/Lead 90%/10%

Note: When mounted with capacitor surface Lc x Tc parallel to the plane of the substrate, the electrodes are perpendicular to the substrate, i.e., in a vertical orientation. This product is packaged in tape-and-reel with the parts in a vertical orientation.

Kit	Description	Values	Tolerance
DKD0708N01	0708N 1.0pF - 10.0pF	1.0, 1.8, 2.2, 3.3, 3.6, 3.9, 4.3, 6.2, 6.8, 7.5, 8.2pF	±.1pF
		10pF	± 5%
DKD0708N02	0708N 10pF - 100pF	10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 39, 43, 47, 68, 100pF	± 5%

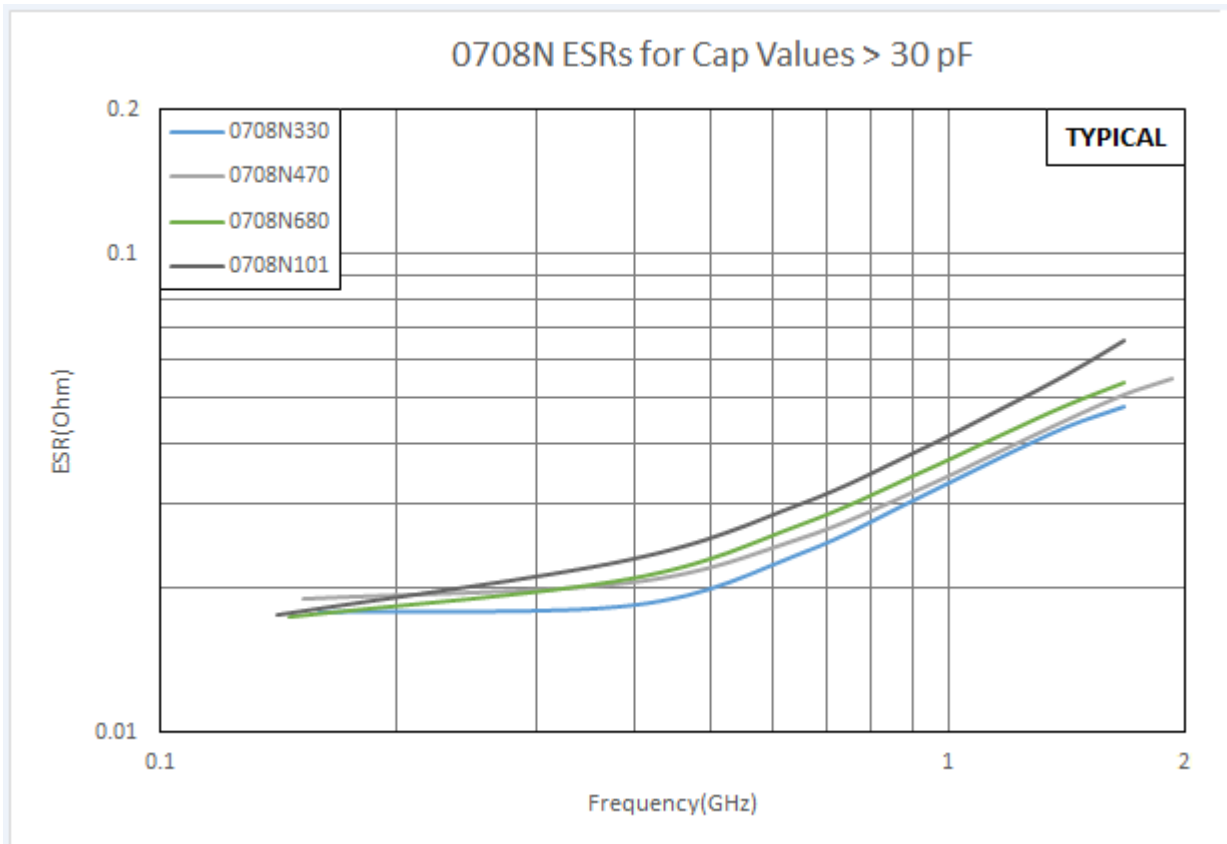
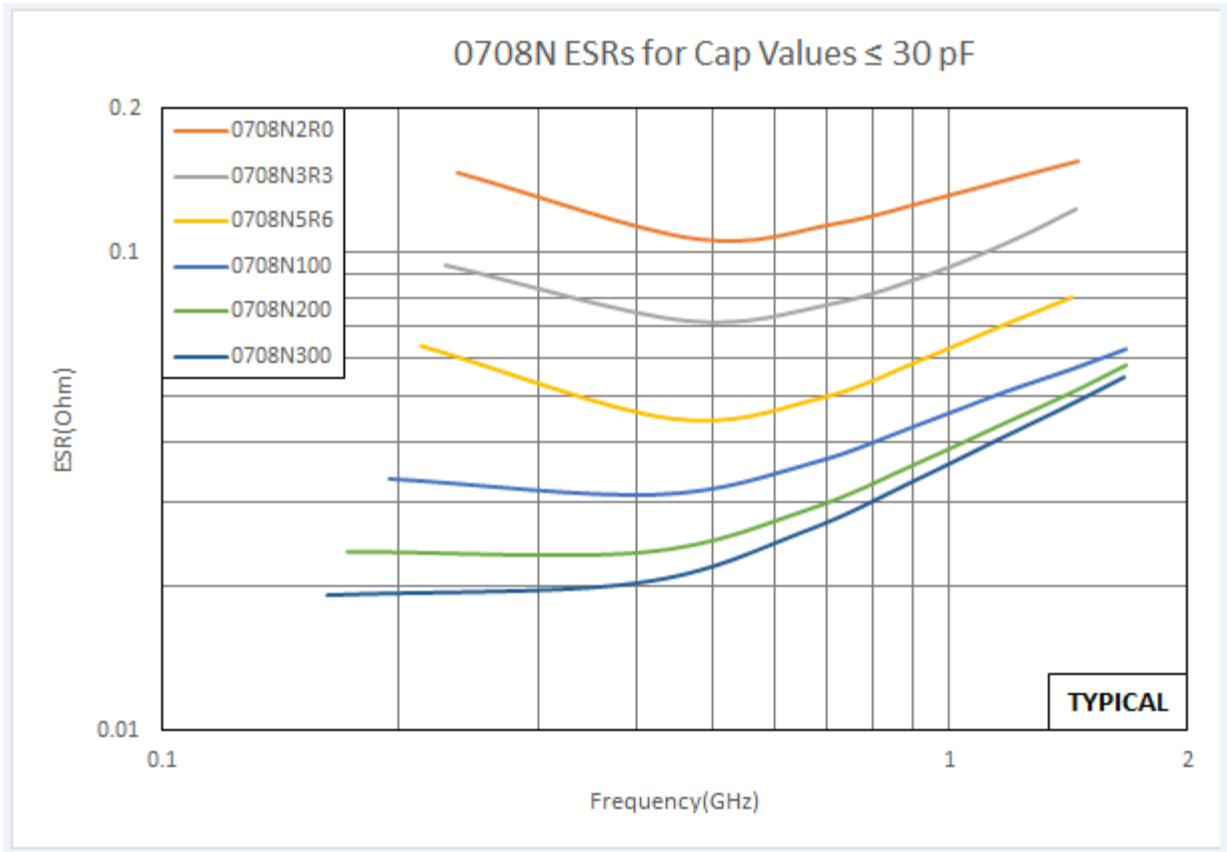
◆ Performance

Item	Specifications
Quality Factor (Q)	2,000 min. @ 1 MHz
Insulation Resistance (IR)	10 ⁵ Megohms min. @ +25 °C at rated WVDC. 10 ⁴ Megohms min. @ +125 °C at rated WVDC.
Rated Voltage	See Capacitance Table
Dielectric Withstanding Voltage (DWV)	250% of Voltage for 5 seconds, Rated Voltage ≤ 500VDC
Operating Temperature Range	-55°C to +175°C
Temperature coefficient (TC)	0 ± 30ppm/°C
Capacitance Drift	± 0.02% or ± 0.02pF, whichever is greater.
Piezoelectric Effects	None

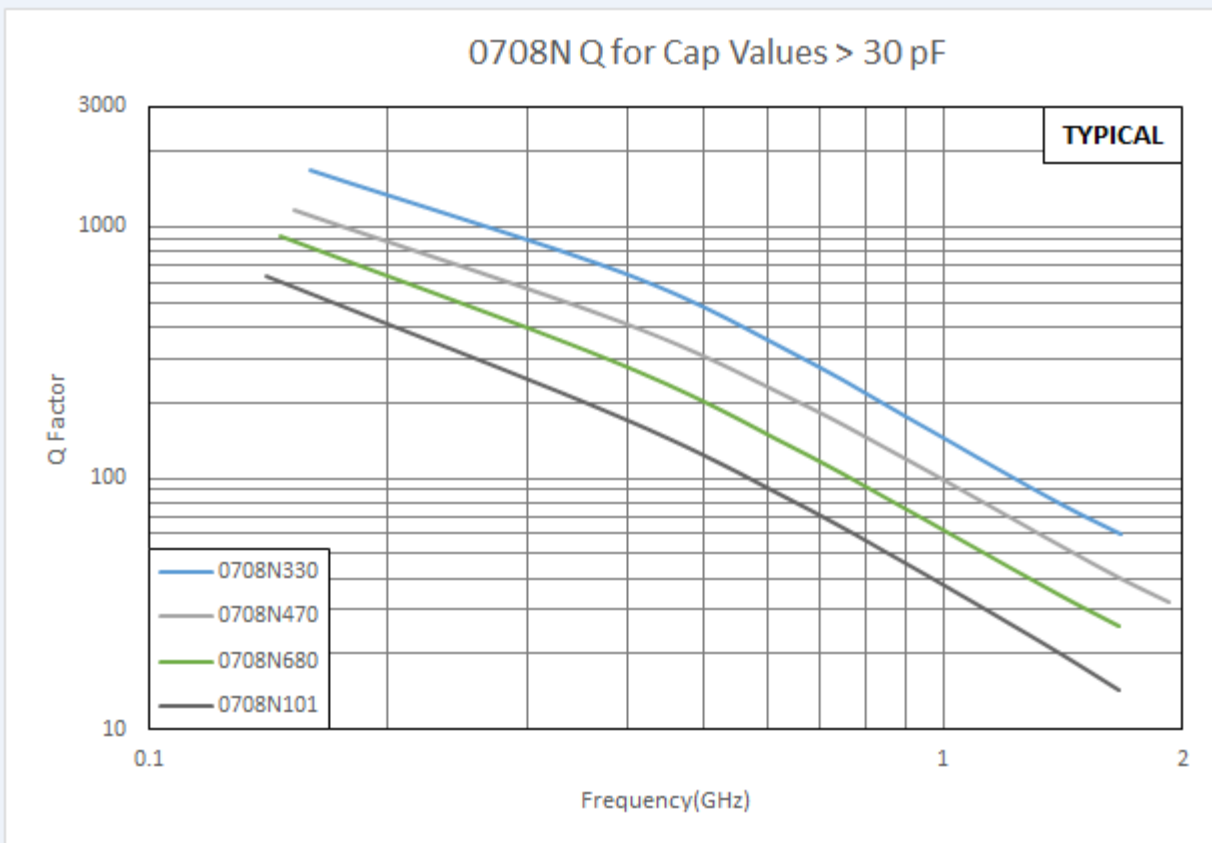
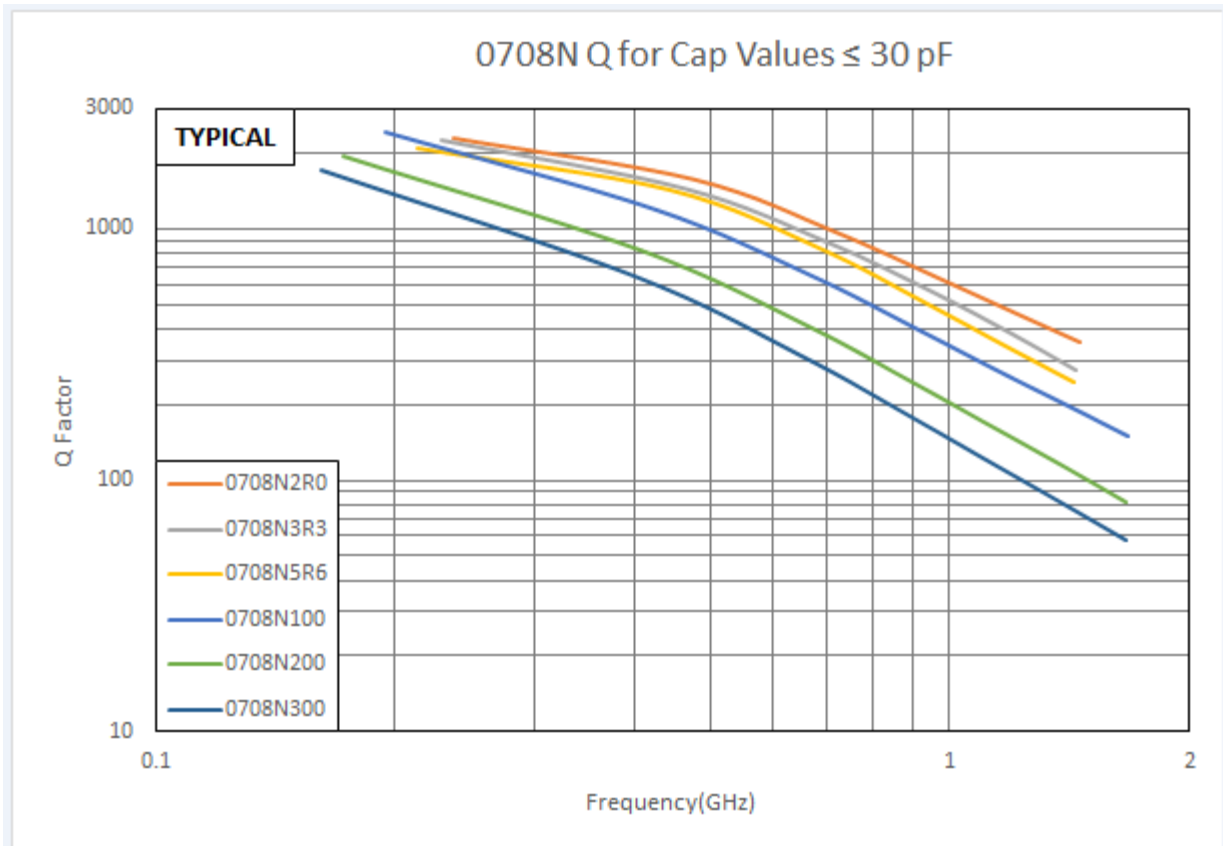
◆ Environmental Tests

Item	Specifications	Method
Terminal Adhesion	Termination should not pull off. Ceramic should remain undamaged.	Terminations for chips withstand a pull of 5 lbs min., 15lbs, typical, for 5 seconds in direction perpendicular to the termination surface of the capacitor. Test per MIL-STD-202, Method 211.
Resistance To soldering heat	No mechanical damage Capacitance change: -1.0% ~ +2.0% Q > 500 I.R. > 10 G Ohms Breakdown voltage: 2.5 x WVDC	Preheat device to 150°C - 180°C for 60 sec. Dip in 260°C ± 5°C solder for 10 ± 1 sec. Measure after 24 ± 2 hour cooling period.
Thermal Shock	No mechanical damage Capacitance change: ± 0.5% or 0.5pF max Q > 500 I.R. > 10 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 107, Condition A. At the maximum rated temperature (-55°C and 175°C) stay 30 minutes. The time of removing shall not be more than 3 minutes. Perform the five cycles.
Humidity, Steady State	No mechanical damage Capacitance change: ± 0.5% or 0.5pF max. Q > 300 I.R. > 1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 106.
Low Voltage Humidity	No mechanical damage Capacitance change: ± 0.3% or 0.3pF max. Q > 300 I.R. > 1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 103, Condition A, with 1.5 Volts D.C. applied while subjected to an environment of 85°C with 85% relative humidity for 240 hours minimum.
Life	No mechanical damage Capacitance change: ± 2.0% or 0.5pF max. Q > 500 I.R. > 1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 108, for 1000 hours, at 175 °C. 200% of Voltage for Capacitors, Rated Voltage ≤ 500VDC

◆ 0708N Electrical Performance Curves - ESR vs. Frequency

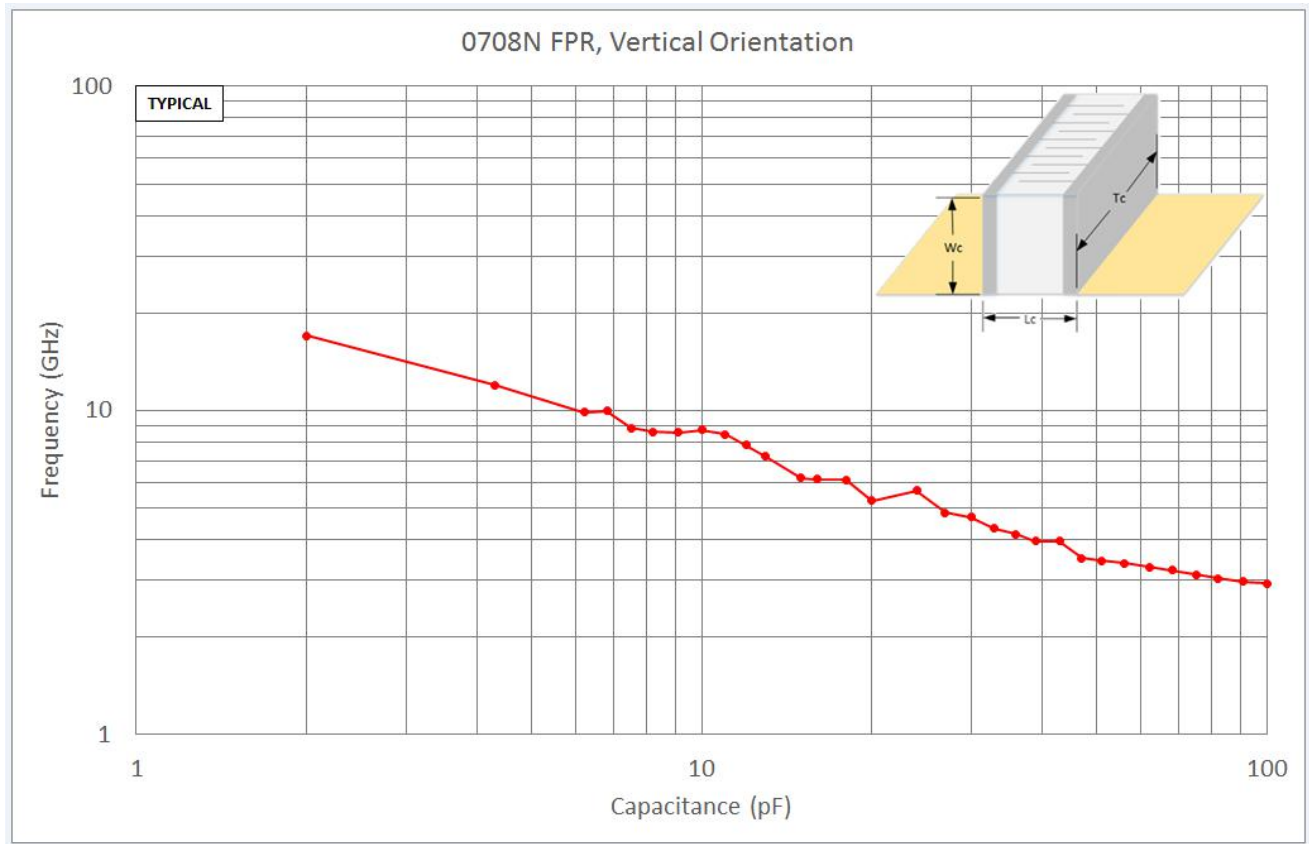


◆ 0708N Electrical Performance Curves - Q Curves



◆ 0708N Electrical Performance Curves

First Parallel Resonant Frequency vs Capacitance
- Vertical Orientation

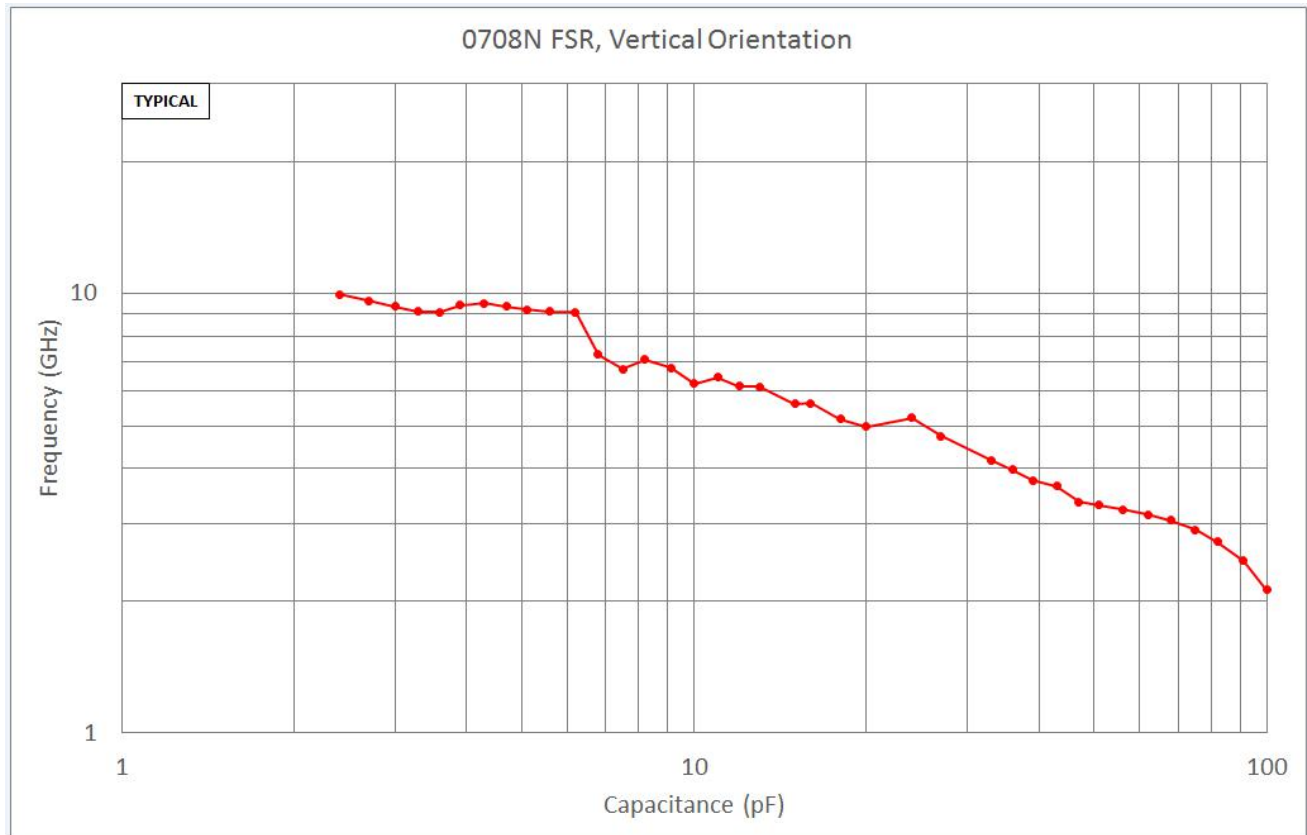


Definitions and Measurement Conditions:

The First Parallel Resonance, FPR, is defined as the lowest frequency at which a suckout or notch appears in (S21). It is generally independent of substrate thickness or dielectric constant, but does depend on capacitor orientation. A vertical orientation means the capacitor electrode planes are perpendicular to the substrate.

◆ 0708N Electrical Performance Curves

First Series Resonant Frequency vs Capacitance
- Vertical Orientation



The First Series Resonance, FSR, is defined as the lowest frequency at which the imaginary part of the input impedance, $\text{Im}[Z_{in}]$, equals zero. Should $\text{Im}[Z_{in}]$ or the real part of the input impedance, $\text{Re}[Z_{in}]$, not be monotonic with frequency at frequencies lower than those at which $\text{Im}[Z_{in}] = 0$, the FSR shall be considered as undefined. FSR is dependent on the internal capacitor structure; substrate thickness and dielectric constant; capacitor orientation, as defined alongside the FPR plot; and mounting pad dimensions.

The definitions on the charts are for a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace with a 50-Ohm termination. The measurement conditions are: substrate - Rogers 3003C; Substrate dielectric constant = 3.0, substrate thickness (mils) = 40; gap in microstrip trace (mils) = 28; microstrip trace width (mils) = 100; Reference planes at sample edges.

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by PPI. The models are derived from measurements on a large number of parts disposed on several different substrates.

S-Parameters can be found on the PPI website—www.passiveplus.com/index.php

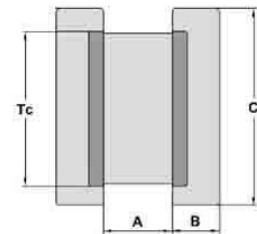
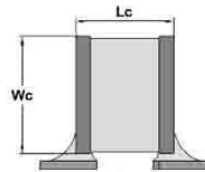
◆ Recommended Land Pattern Dimensions

When mounting the capacitor to substrate, it's important to carefully consider that the amount of solder (size of fillet) used has a direct effect upon the capacitor once it's mounted.

- 1) The greater the amount of solder, the greater the stress to the elements. This may cause the substrate to break or crack.
- 2) In the situation where two or more devices are mounted onto a common land, be sure to separate the device into exclusive pads by using soldering resist.

● Vertical Mounting Dimensions: mm

Orientation	EIA	A	B	C
Vertical	0708	0.71	1.00	2.90



Lc = Length of Capacitor
Wc = Width of Capacitor
Tc = Thickness of Capacitor

◆ Tape & Reel Specifications - Vertical Orientation Dimensions: mm

Orientation	EIA	A0	B0	K0	W	P0	P1	T	F	QTY Min	QTY/ REEL	Tape Material
Vertical	0708N	1.90	2.65	2.20	12.00	4.00	4.00	0.30	5.50	500	1500	Plastic

