# C4H2327N110A

**AMPLEON** 

Power GaN transistor
Rev. 1 — 23 December 2021

Product data sheet

#### **Product profile** 1.

### 1.1 General description

100 W GaN packaged Doherty power transistor for base station applications at frequencies from 2300 MHz to 2700 MHz.

**Typical performance** 

Typical RF performance at T<sub>case</sub> = 25 °C in a Doherty application demo circuit, unless otherwise specified.

Test signal	$I_{Dq}$	V <sub>DS</sub>	V <sub>GS(amp)peak</sub>	P <sub>L(AV)</sub>	Gp	ηр	ACPR	P <sub>L(5dB)</sub>			
	(mA)	(V)	(V)	(dBm)	(dB)	(%)	(dBc)	(dBm)			
f = 2300 MHz to 2400 MH	f = 2300 MHz to 2400 MHz										
1-carrier W-CDMA [1]	40	50	-7.0	41.5	14.9	57.1	-24.8	-			
pulsed CW [2]	40	50	-7.0	-	-	-	-	50.5			
f = 2496 MHz to 2690 MH	lz										
1-carrier W-CDMA [1]	50	50	-5.1	41.5	15.0	57.0	-27.1	-			
pulsed CW [2]	50	50	<b>-5.1</b>	-	-	-	-	50.5			

<sup>[1]</sup> Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 10.5 dB at 0.01 % probability on CCDF.

#### 1.2 Features and benefits

- Excellent digital pre-distortion capability
- High efficiency
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

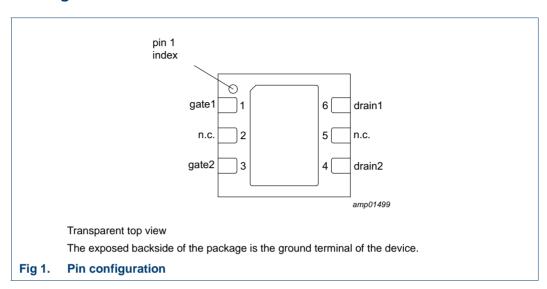
### 1.3 Applications

■ RF power amplifier for base stations and multi carrier applications in the 2300 MHz to 2700 MHz frequency range

<sup>[2]</sup> Test signal: pulsed CW;  $t_p = 30 \mu s$ ;  $\delta = 35 \%$ .

### 2. Pinning information

### 2.1 Pinning



### 2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
gate1	1	gate 1
n.c.	2	not connected
gate2	3	gate 2
drain2	4	drain 2
n.c.	5	not connected
drain1	6	drain 1

### 3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
DFN-7x6.5-6-1	C4H2327N110AZ	9349 604 22515	TR7; 1000-fold; 16 mm; dry pack	1000
	C4H2327N110AX	9349 604 22525	TR13; 3000-fold; 16 mm; dry pack	3000

### 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage	operating	-	52	V
V <sub>DS</sub>	drain-source voltage	$V_{GS} = -8 \text{ V}$	-	150	V
V <sub>GS(amp)main</sub>	main amplifier gate-source voltage		-15	+2	V
V <sub>GS(amp)peak</sub>	peak amplifier gate-source voltage		-15	+2	V
I <sub>GF(amp)main</sub>	main amplifier forward gate current		-	4.8	mΑ
I <sub>GF(amp)peak</sub>	peak amplifier forward gate current		-	7.2	mΑ
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>ch</sub>	active die channel temperature	[1]	-	275	°C
T <sub>case</sub>	case temperature	operating [1]	-40	+140	°C

<sup>[1]</sup> Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R <sub>th(s-c)(IR)</sub> [1]	thermal resistance from active die surface to case by Infrared measurement	$T_{case} = 90 ^{\circ}\text{C};  P_{dis(main)} = 9  \text{W};$ $P_{dis(peak)} = 2.5  \text{W}$	4.00	K/W
R <sub>th(ch-c)(FEA)</sub> [2]	thermal resistance from active die channel to case by Finite Element Analysis	$T_{case} = 90  ^{\circ}\text{C};  P_{dis(main)} = 9  \text{W};$ $P_{dis(peak)} = 2.5  \text{W}$	6.20	K/W

<sup>[1]</sup> Infrared (IR) thermal values are for reference only and cannot be used to determine performance or reliability.

### 6. Characteristics

Table 6. DC characteristics

 $T_i = 25$  °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit					
Main dev	Main device										
V <sub>GS(th)</sub>	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_D = 4.8 \text{ mA}$	-3.27	-2.87	-2.47	V					
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 48 \text{ V}; I_D = 96 \text{ mA}$	-3.02	-2.62	-2.22	V					
I <sub>D(leak)</sub>	drain leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 50 \text{ V}$	-	-	1.16	mΑ					
I <sub>GSS</sub>	gate leakage current	$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	0.23	mΑ					
Peak dev	vice										
V <sub>GS(th)</sub>	gate-source threshold voltage	$V_{DS} = 10 \text{ V}; I_D = 7.2 \text{ mA}$	-3.20	-2.80	-2.40	V					
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 48 \text{ V}; I_D = 144 \text{ mA}$	-3.02	-2.62	-2.22	V					
I <sub>D(leak)</sub>	drain leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 50 \text{ V}$	-	-	1.74	mΑ					
I <sub>GSS</sub>	gate leakage current	$V_{GS} = -8 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	0.35	mΑ					

<sup>[2]</sup> Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

#### Table 7. RF characteristics

Test signal: pulsed CW;  $t_p = 50~\mu s$ ;  $\delta = 1.38~\%$ ;  $f_1 = 2496~MHz$ ;  $f_2 = 2690~MHz$ ; RF performance at  $V_{DS} = 48~V$ ;  $I_{Dq1} = 50~mA$ ;  $I_{Dq2} = 70~mA$ ;  $T_{case} = 25~^{\circ}\text{C}$ ; unless otherwise specified; in a class-AB production RF test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Main dev	rice					
Gp	power gain	P <sub>L(AV)</sub> = 14.1 W	16.0	18.2	-	dB
$\eta_{D}$	drain efficiency	P <sub>L(AV)</sub> = 14.1 W	32.0	36.0	-	%
P <sub>L(3dB)</sub>	output power at 3 dB gain compression		43.0	46.0	-	dBm
Peak dev	rice					
Gp	power gain	P <sub>L(AV)</sub> = 14.1 W	16.0	18.5	-	dB
$\eta_{D}$	drain efficiency	P <sub>L(AV)</sub> = 14.1 W	27.0	31.0	-	%
P <sub>L(3dB)</sub>	output power at 3 dB gain compression		43.0	47.0	-	dBm

### 7. Test information

### 7.1 Ruggedness in Doherty operation

### 7.1.1 At f = 2300 MHz; tested on the Doherty application demo board

The C4H2327N110A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 30 \text{ mA}$ ;  $V_{GS(amp)peak} = -5.6 \text{ V}$ ;  $P_{L} = 100 \text{ W}$  (pulsed CW;  $t_p = 100 \text{ µs}$ ;  $\delta = 10 \text{ %}$ ).

### 7.1.2 At f = 2496 MHz; tested on the Doherty development RF test circuit

The C4H2327N110A is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS}$  = 50 V;  $I_{Dq}$  = 50 mA;  $V_{GS(amp)peak}$  = -5.3 V;  $P_{L}$  = 95 W (pulsed CW;  $t_p$  = 100  $\mu$ s;  $\delta$  = 10 %).

### 7.2 Impedance information

#### Table 8. Typical impedance of maximum power and drain efficiency

Measured load-pull data (main device); all data measured on a harmonic impedance optimized load-pull fixture;  $I_{Dq} = 45$  mA;  $V_{DS} = 50$  V; test signal: pulsed CW;  $t_p = 100$   $\mu$ s;  $\delta = 10$  %; typical values unless otherwise specified.

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]		η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	<b>(</b> Ω <b>)</b>	<b>(</b> Ω <b>)</b>	dBm)	(W)	(%)	(dB)
Maximum p	ower load					
2300	7.0 – j16.0	13.7 + j9.7	47.3	54	67.4	18.9
2350	7.0 – j16.0	14.7 + j8.0	47.4	55	65.5	18.5
2400	7.0 – j16.0	15.7 + j8.7	47.4	55	67.6	18.7
2500	14.0 – j35.1	12.8 + j9.1	47.2	52	68.0	18.7
2600	28.8 – j47.6	12.8 + j9.0	47.4	55	67.0	17.8
2700	89.5 – j56.8	12.8 + j9.1	47.1	51	69.0	17.6
Maximum o	drain efficiency load					
2300	7.0 – j16.0	12.1 + j16.9	46.2	42	77.5	20.6
2350	7.0 – j16.0	10.4 + j18.2	45.3	34	78.1	21.3

Table 8. Typical impedance of maximum power and drain efficiency ...continued

Measured load-pull data (main device); all data measured on a harmonic impedance optimized load-pull fixture;  $I_{Dq} = 45$  mA;  $V_{DS} = 50$  V; test signal: pulsed CW;  $t_p = 100$   $\mu$ s;  $\delta = 10$  %; typical values unless otherwise specified.

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]		η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	<b>(</b> Ω <b>)</b>	<b>(</b> Ω <b>)</b>	dBm)	(W)	(%)	(dB)
2400	7.0 – j16.0	9.1 + j16.8	45.6	36	77.9	21.7
2500	14.0 – j35.1	8.5 + j14.7	46.0	40	80.0	20.9
2600	28.8 – j47.6	10.2 + j15.5	46.0	40	78.7	19.0
2700	89.5 – j56.8	9.4 + j15.8	45.7	37	79.6	18.9

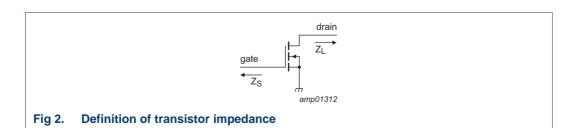
- [1] Z<sub>S</sub> and Z<sub>L</sub> defined in Figure 2.
- [2] At 3 dB gain compression.

Table 9. Typical impedance of maximum power and drain efficiency

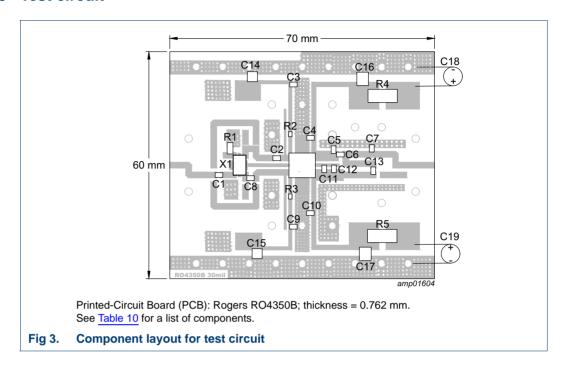
Measured load-pull data (peak device); all data measured on a harmonic impedance optimized load-pull fixture;  $I_{Dq}$  = 70 mA;  $V_{DS}$  = 50 V; test signal: pulsed CW;  $t_p$  = 100  $\mu$ s;  $\delta$  = 10 %; typical values unless otherwise specified.

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]	P <sub>L</sub> [2]		η <sub>D</sub> [2]	G <sub>p</sub> [2]
(MHz)	<b>(</b> Ω <b>)</b>	<b>(</b> Ω <b>)</b>	(dBm)	(W)	(%)	(dB)
Maximun	n power load		'	,		
2300	4.8 – j7.6	10.0 + j5.7	49.5	90	67.7	18.5
2350	4.8 – j7.6	7.9 + j6.9	49.6	91	70.7	19.5
2400	4.8 – j7.6	7.8 + j6.8	49.5	90	70.2	20.4
2500	3.1 – j9.5	8.8 + j4.7	49.3	85	64.5	18.3
2600	7.5 – j15.7	8.5 + j5.8	49.3	83	66.1	18.8
2700	6.4 – j8.9	7.4 + j5.4	49.2	84	64.3	17.7
Maximun	n drain efficiency	load	<u>'</u>			
2300	4.8 – j7.6	6.2 + j10.3	48.8	76	76.4	19.9
2350	4.8 – j7.6	7.3 + j11.9	47.9	61	77.6	20.9
2400	4.8 – j7.6	7.6 + j11.6	47.9	61	76.6	21.8
2500	3.1 – j9.5	6.5 + j9.8	47.9	61	76.3	19.8
2600	7.5 – j15.7	6.5 + j9.8	48.0	63	74.7	20.1
2700	6.4 – j8.9	6.4 + j9.8	48.1	64	74.3	18.5

- [1]  $Z_S$  and  $Z_L$  defined in Figure 2.
- [2] At 3 dB gain compression.



### 7.3 Test circuit



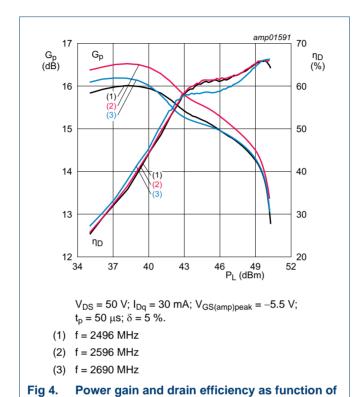
**Table 10.** List of components
See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C3, C9	multilayer ceramic chip capacitor	8.2 pF	ATC 600F
C2, C8	multilayer ceramic chip capacitor	1.8 pF	ATC 600F
C4	multilayer ceramic chip capacitor	7.5 pF	ATC 600F
C5	multilayer ceramic chip capacitor	1.2 pF	ATC 600F
C6, C13	multilayer ceramic chip capacitor	1.5 pF	ATC 600F
C7	multilayer ceramic chip capacitor	0.9 pF	ATC 600F
C10	multilayer ceramic chip capacitor	7.5 pF	ATC 600F
C11	multilayer ceramic chip capacitor	2.0 pF	ATC 600F
C12	multilayer ceramic chip capacitor	0.3 pF	ATC 600F
C14, C15	multilayer ceramic chip capacitor	10 μF, 100 V	Murata: GRM32EC72A106KE05L
C16, C17	multilayer ceramic chip capacitor	10 μF, 100 V	Murata: KRM55QR72A106KH01L
C18, C19	electrolytic capacitor	1000 μF, 100 V	Murata
R1	resistor	51 Ω	SMD 0805
R2, R3	resistor	5.1 Ω	SMD 0603
R4, R5	high precision current sense resistor	0.1 Ω	Bourns: CRM2512-FX-R100ELF
X1	hybrid coupler	2 dB, 90°	Anaren: X3C25F1-02S

### 7.4 Graphical data

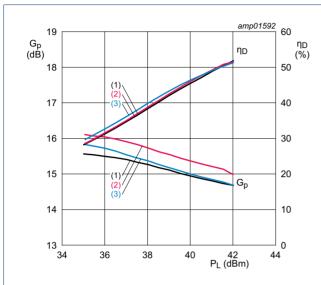
All the data are measured on the Doherty RF test circuit.

#### 7.4.1 Pulsed CW



output power; typical values

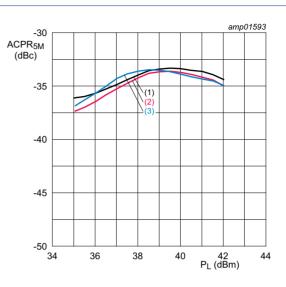
#### 7.4.2 1-Carrier W-CDMA



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 30 mA;  $V_{GS(amp)peak}$  = -5.5 V.

- (1) f = 2496 MHz
- (2) f = 2596 MHz
- (3) f = 2690 MHz

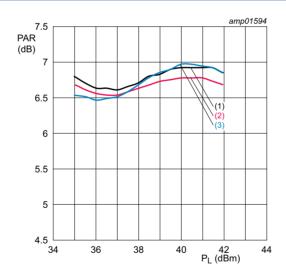
Fig 5. Power gain and drain efficiency as function of average output power; typical values



 $V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 30 \text{ mA}$ ;  $V_{GS(amp)peak} = -5.5 \text{ V}$ .

- (1) f = 2496 MHz
- (2) f = 2596 MHz
- (3) f = 2690 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

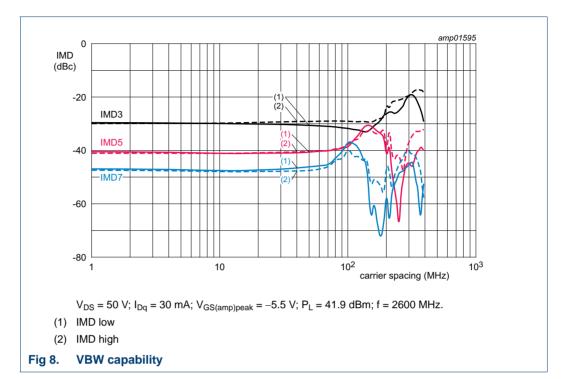


 $V_{DS} = 50 \text{ V}; I_{Dq} = 30 \text{ mA}; V_{GS(amp)peak} = -5.5 \text{ V}.$ 

- (1) f = 2496 MHz
- (2) f = 2596 MHz
- (3) f = 2690 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

### 7.4.3 2-Tone VBW



### 8. Package outline

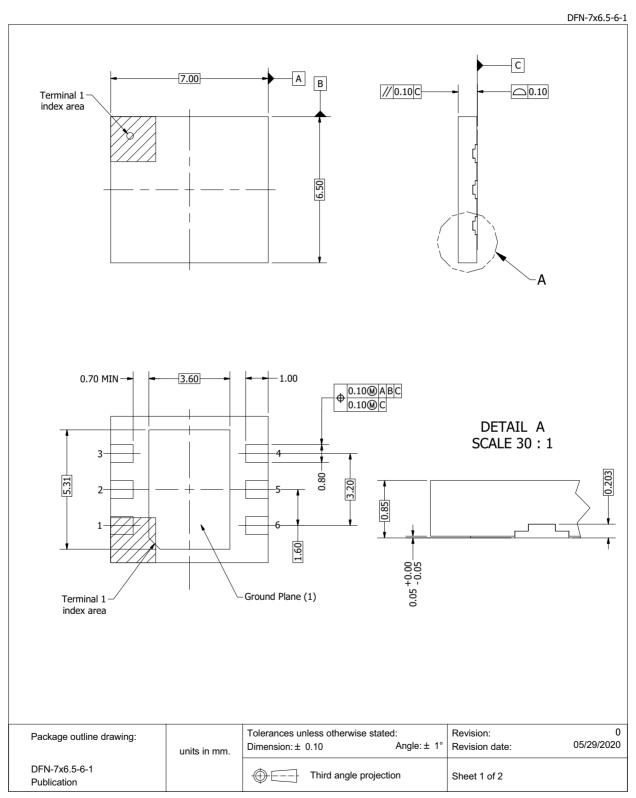


Fig 9. Package outline DFN-7x6.5-6-1 (sheet 1 of 2)

DFN-7x6.5-6-1

						BITT 7X015
			Drawing Notes			
tems			Description			
(1)	Terminals (bottom View) a	and ground-plane	(bottom View) are plated with matte	Sn.		
(2)			ax. per side are not included.			
. ,	гисте стительный развительный		рег сис и с постинения			
			Tolerances unless otherwise stated	1.	Revision:	
Packa	age outline drawing:		1			05/29/202
		units in mm.	Dimension: ± 0.10	Angle: ± 1°	Revision date:	05/29/202
DFN-	-7x6.5-6-1		Third angle projection	nn.	Sheet 2 of 2	
	cation			JI I	LOUBEL / UL /	

Fig 10. Package outline DFN-7x6.5-6-1 (sheet 2 of 2)

### 9. Handling information

#### **CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A [2]

- [1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.
- [2] HBM classification 1A is granted to any part that passes after exposure to an ESD pulse of 250 V.

### 10. Abbreviations

Table 12. Abbreviations

Acronym	Description		
3GPP	3rd Generation Partnership Project		
CCDF	Complementary Cumulative Distribution Function		
CW	Continuous Wave		
DPCH	Dedicated Physical CHannel		
GaN	Gallium Nitride		
MTF	Median Time to Failure		
PAR	Peak-to-Average Ratio		
RoHS	Restriction of Hazardous Substances		
SMD	Surface Mounted Device		
VBW	Video BandWidth		
VSWR	Voltage Standing Wave Ratio		
W-CDMA	Wideband Code Division Multiple Access		

### 11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
C4H2327N110A v.1	20211223	Product data sheet	-	-

### 12. Legal information

#### 12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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### 13. Contact information

For more information, please visit: http://www.ampleon.com

For sales office addresses, please visit: http://www.ampleon.com/sales

## C4H2327N110A

### **Power GaN transistor**

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