

1. Product profile

1.1 General description

10 W GaN packaged power transistor for base station applications.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a class-AB application demo circuit; unless otherwise specified.

Test signal	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (dBm)	G_p (dB)	η_D (%)	ACPR (dBc)	$P_{L(5dB)}$ (dBm)
f = 2300 MHz to 2400 MHz							
1-carrier W-CDMA [1]	10	50	27	20.5	13.9	-35.9	-
pulsed CW [2]	10	50	-	-	-	-	40.4
f = 2496 MHz to 2690 MHz							
1-carrier W-CDMA [1]	10	50	27	18.9	15.5	-36.3	-
pulsed CW [2]	10	50	-	-	-	-	40.5
f = 3400 MHz to 3600 MHz							
1-carrier W-CDMA [1]	10	50	27	19.4	16.6	-34.7	-
pulsed CW [2]	10	50	-	-	-	-	40.5

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 10.5 dB at 0.01 % probability on CCDF.

[2] Test signal: pulsed CW; $t_p = 30\text{ }\mu\text{s}$; $\delta = 35\text{ }\%$.

1.2 Features and benefits

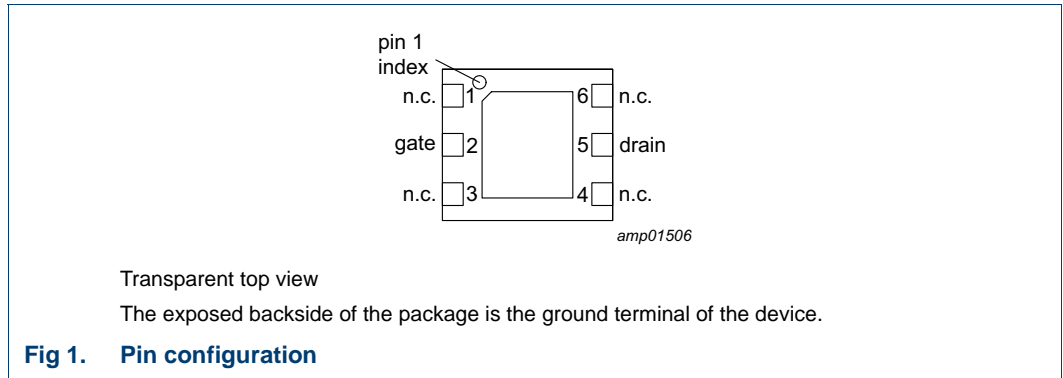
- Excellent digital pre-distortion capability
- High efficiency
- Designed for broadband operation
- Lower output capacitance for improved performance in applications
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 2300 MHz to 5000 MHz frequency range

2. Pinning information

2.1 Pinning



2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	1	not connected
gate	2	gate
n.c.	3	not connected
n.c.	4	not connected
drain	5	drain
n.c.	6	not connected

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
DFN-4.5x4-6-1	C4H2350N10X	9349 604 23525	TR13; 3000-fold; 12 mm; dry pack	3000
	C4H2350N10Z	9349 604 23515	TR7; 1000-fold; 12 mm; dry pack	1000

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage	operating	-	52	V
V _{DS}	drain-source voltage	V _{GS} = -8 V	-	150	V
V _{GS}	gate-source voltage		-15	+2	V
I _{GF}	forward gate current		-	1.1	mA
T _{stg}	storage temperature		-65	+150	°C
T _{ch}	active die channel temperature	[1]	-	275	°C
T _{case}	case temperature	operating [1]	-40	+140	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(s-c)(IR)} [1]	thermal resistance from active die surface to case by Infrared measurement	T _{case} = 105 °C; P _{dis} = 4.8 W	8.70	K/W
R _{th(ch-c)(FEA)} [2]	thermal resistance from active die channel to case by Finite Element Analysis	T _{case} = 105 °C; P _{dis} = 4.8 W	15.40	K/W

[1] Infrared (IR) thermal values are for reference only and cannot be used to determine performance or reliability.

[2] Finite Element Analysis (FEA) thermal values have been used for the online MTF calculator.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 1.10 mA	-3.31	-2.91	-2.51	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 50 V; I _D = 11 mA	-3.05	-2.65	-2.25	V
I _{D(leak)}	drain leakage current	V _{GS} = -10 V; V _{DS} = 50 V	-	-	0.24	mA
I _{GSS}	gate leakage current	V _{GS} = -8 V; V _{DS} = 0 V	-	-	0.05	mA

Table 7. RF characteristics

Test signal: pulsed CW; t_p = 50 μs; δ = 1.38 %; f₁ = 2496 MHz; f₂ = 2690 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 10 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G _p	power gain	P _{L(AV)} = 0.251 W	14.5	18.6	-	dB
η _D	drain efficiency	P _{L(AV)} = 0.251 W	7.0	12.0	-	%
P _{L(3dB)}	output power at 3 dB gain compression		4.5	10.4	-	W

7. Test information

7.1 Ruggedness in Doherty operation

7.1.1 At f = 2300 MHz; tested on the class-AB application demo board

The C4H2350N10 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{Dq} = 10\text{ mA}$; $P_L = 10\text{ W}$ (pulsed CW; $t_p = 12\text{ }\mu\text{s}$; $\delta = 10\%$).

7.1.2 At f = 2496 MHz; tested on the class-AB RF test circuit

The C4H2350N10 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{Dq} = 10\text{ mA}$; $P_L = 8\text{ W}$ (pulsed CW; $t_p = 50\text{ }\mu\text{s}$; $\delta = 10\%$).

7.1.3 At f = 3400 MHz; tested on the class-AB application demo board

The C4H2350N10 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{Dq} = 15\text{ mA}$; $P_L = 10\text{ W}$ (pulsed CW; $t_p = 12\text{ }\mu\text{s}$; $\delta = 10\%$).

7.2 Impedance information

Table 8. Typical impedance of maximum power and drain efficiency

Measured load-pull data; all data measured on a harmonic impedance non-optimized load-pull fixture; $I_{Dq} = 10\text{ mA}$; $V_{DS} = 50\text{ V}$; test signal: pulsed CW; $t_p = 50\text{ }\mu\text{s}$; $\delta = 10\%$; typical values unless otherwise specified.

f	Z _S [1]	Z _L [1]	P _L [2]		η _D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(dBm)	(W)	(%)	(dB)
Maximum power load						
2500	10.0 + j17.4	42.8 + j41.2	40.4	11	59.6	17.9
2600	9.7 + j15.3	50.6 + j41.4	40.4	11	59.2	17.4
2700	9.4 + j12.8	50.6 + j41.4	40.4	11	59.1	17.2
3400	3.9 – j7.2	50.6 + j46.6	40.4	11	59.1	15.1
3500	3.9 – j7.2	52.3 + j44.0	40.0	10	57.9	15.2
3600	3.9 – j7.2	50.0 + j44.0	40.0	10	57.3	15.1
Maximum drain efficiency load						
2500	10.0 + j17.4	38.3 + j69.4	39.5	9	69.0	17.7
2600	9.7 + j15.3	39.7 + j75.9	39.0	8	67.1	17.7
2700	9.4 + j12.8	34.9 + j58.4	39.5	9	66.8	18.3
3400	3.9 – j7.2	35.7 + j63.5	40.0	10	68.9	14.8
3500	3.9 – j7.2	20.4 + j62.0	38.5	7	69.0	15.0
3600	3.9 – j7.2	21.0 + j54.0	39.0	8	69.4	15.8

[1] Z_S and Z_L defined in [Figure 2](#).

[2] At 3 dB gain compression.

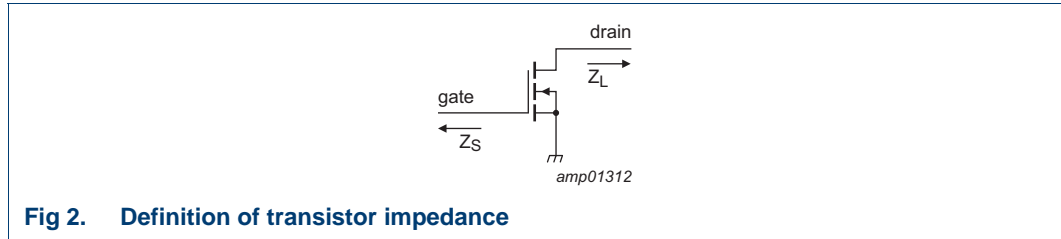
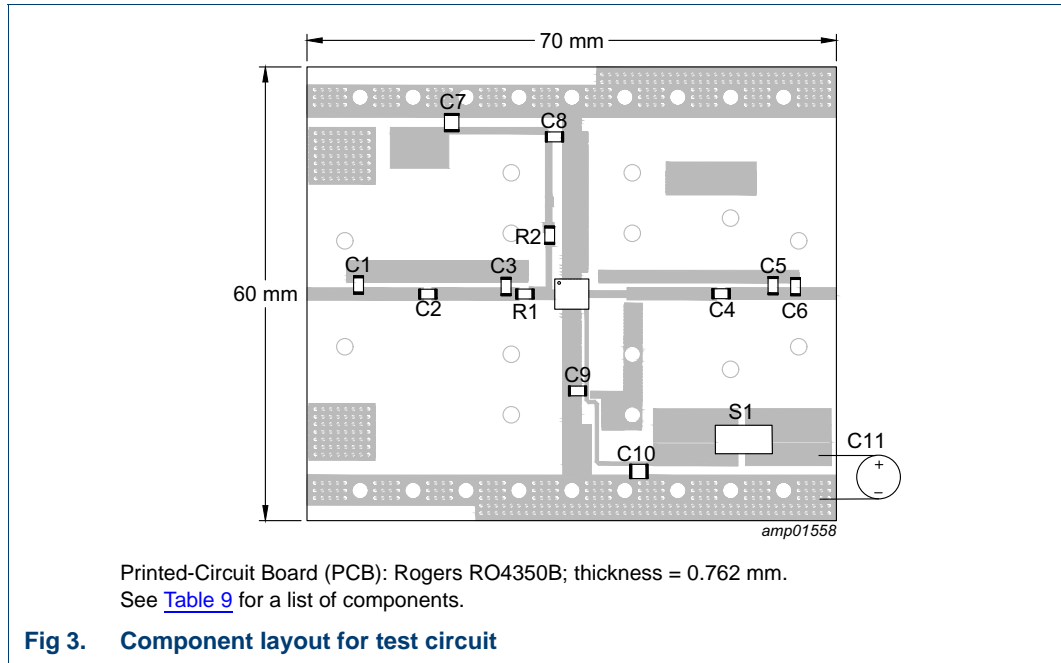


Fig 2. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.762 mm.
See [Table 9](#) for a list of components.

Fig 3. Component layout for test circuit

Table 9. List of components

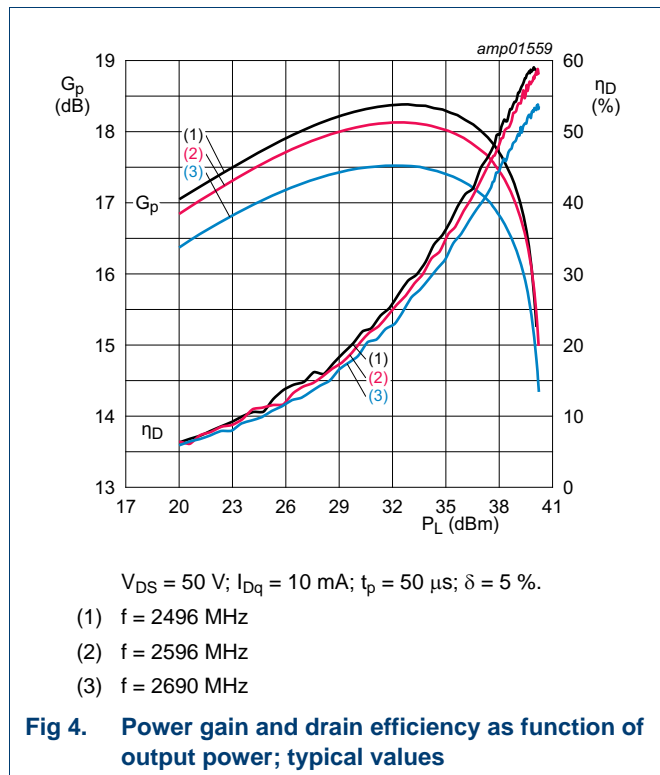
See [Figure 3](#) for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	0.8 pF	ATC 600F
C2, C8, C9	multilayer ceramic chip capacitor	10 pF	ATC 600F
C3	multilayer ceramic chip capacitor	1.5 pF	ATC 600F
C4	multilayer ceramic chip capacitor	20 pF	ATC 600F
C5	multilayer ceramic chip capacitor	0.1 pF	ATC 600F
C6	multilayer ceramic chip capacitor	0.5 pF	ATC 600F
C7	multilayer ceramic chip capacitor	10 μ F, 100 V	Murata: GRM32EC72A106KE05L
C10	multilayer ceramic chip capacitor	10 μ F, 100 V	Murata: KRM55QR72A106KH01L
C11	electrolytic capacitor	1000 μ F, 100 V	Murata
R1, R2	resistor	5.1 Ω	SMD 0603
S1	high precision current sense resistor	0.1 Ω	Bourns: CRM2512-FX-R100ELF

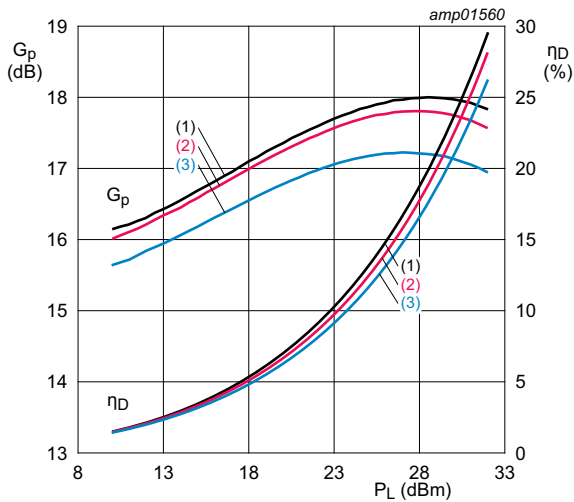
7.4 Graphical data

All the data are measured on the class-AB RF test circuit.

7.4.1 Pulsed CW

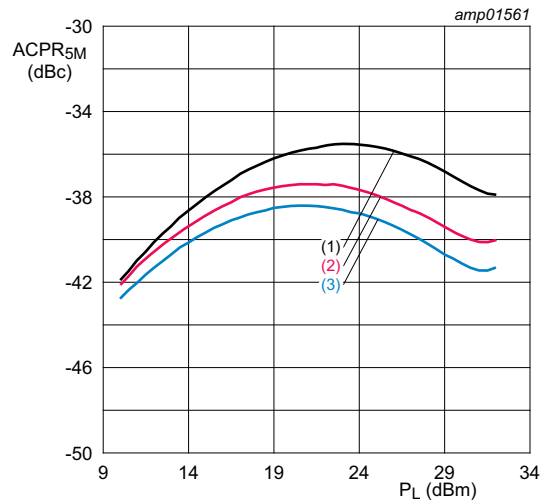


7.4.2 1-Carrier W-CDMA



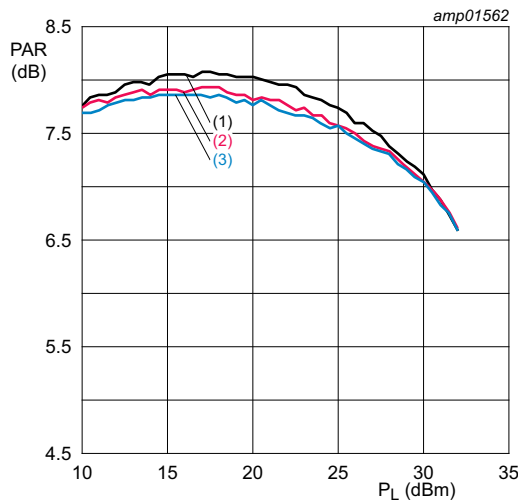
$V_{DS} = 50\text{ V}; I_{Dq} = 10\text{ mA}.$
 (1) $f = 2496\text{ MHz}$
 (2) $f = 2596\text{ MHz}$
 (3) $f = 2690\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of average output power; typical values



$V_{DS} = 50\text{ V}; I_{Dq} = 10\text{ mA}.$
 (1) $f = 2496\text{ MHz}$
 (2) $f = 2596\text{ MHz}$
 (3) $f = 2690\text{ MHz}$

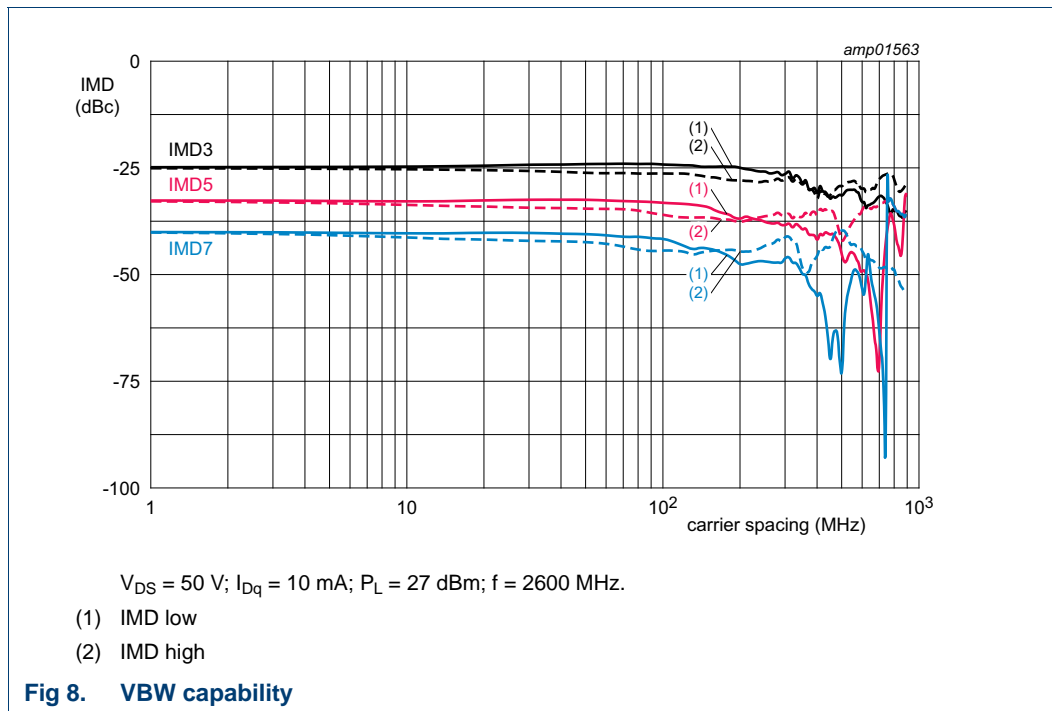
Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



$V_{DS} = 50\text{ V}; I_{Dq} = 10\text{ mA}.$
 (1) $f = 2496\text{ MHz}$
 (2) $f = 2596\text{ MHz}$
 (3) $f = 2690\text{ MHz}$

Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Tone VBW



8. Package outline

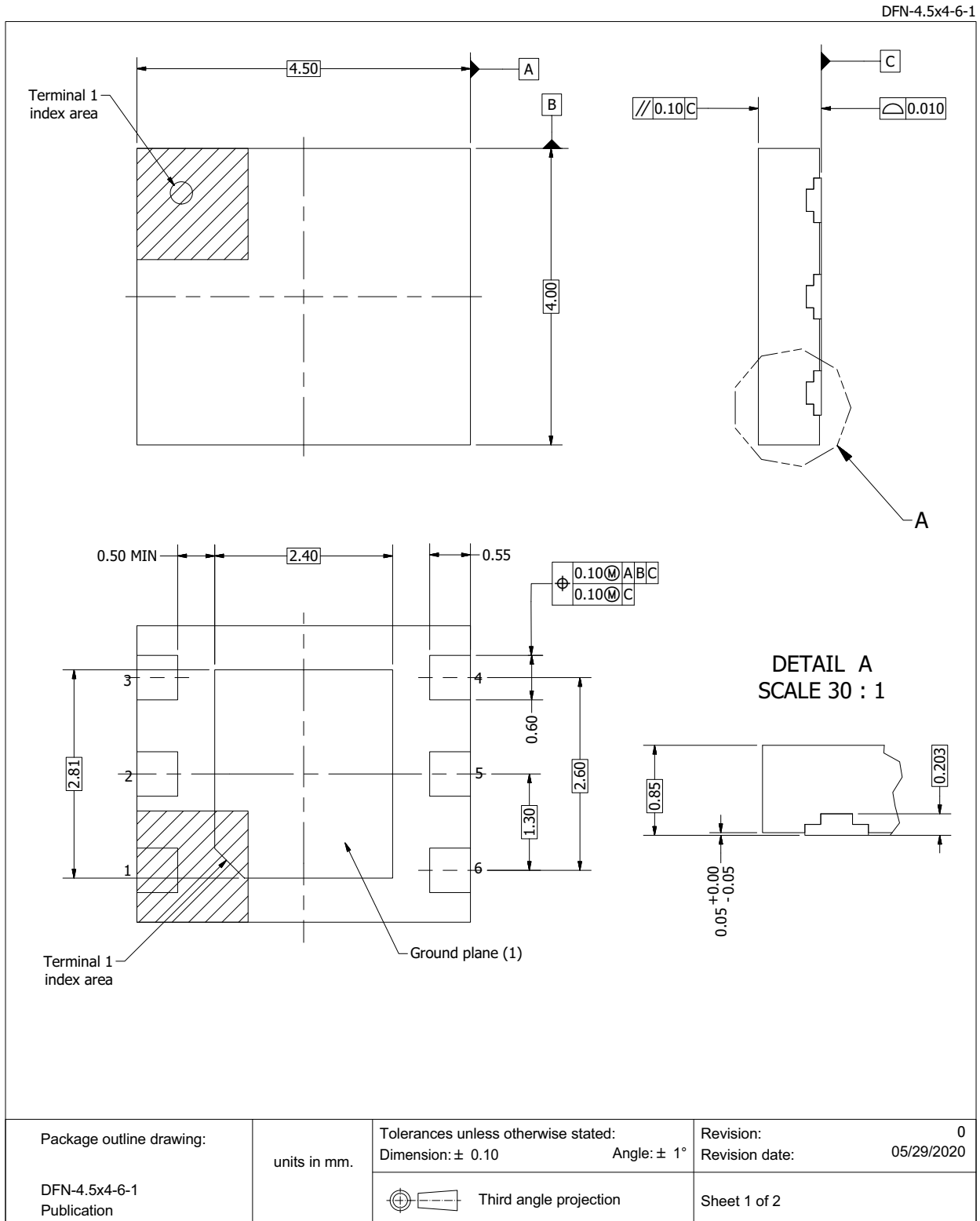


Fig 9. Package outline DFN-4.5x4-6-1 (sheet 1 of 2)

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A [2]

[1] CDM classification C2A1 is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 1A is granted to any part that passes after exposure to an ESD pulse of 250 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
GaN	Gallium Nitride
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
C4H2350N10 v.1	20211223	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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