

Surface Mount 10 W High Power Amplifier

17-20.5 GHz



Product Datasheet

K-HPA10W-1721-SM

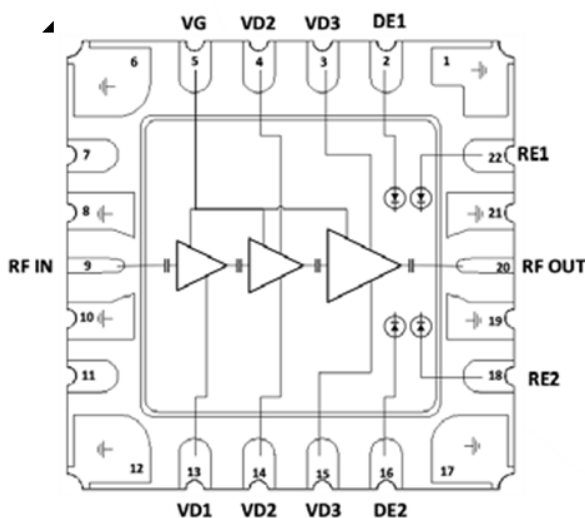
Surface Mount 10 W GaN MMIC High Power Amplifier for K-band.

Overview

K-HPA10W-1721-SM is a High Power MMIC Amplifier fabricated on Space Qualified 0.25 μm GaN on SiC. This MMIC operates from 17-20.5 GHz and delivers >10 W saturated output power across the band, with power-added efficiency in excess of 25% and large-signal gain of 20 dB.

The part is offered in a 7x7 mm hermetically sealed surface mount ceramic package and is matched to 50 Ω with integrated DC blocking capacitors on RF ports. The part incorporates an output power detector to assist with system integration and is well suited for satellite communications and point to point applications.

Functional Diagram



Features

- Frequency range 17-20.5 GHz
- Power >10 W saturated
- Small signal gain 25 dB
- Large signal gain 20 dB
- Integrated power detector
- PAE: >25% at Pin=20 dBm
- Bias: VD=25 V, IDQ=300 mA, VG=3.6 V
- QFN dimensions 7x7 mm



Applications

- Satellite communications
- Radar
- Mobile communications
- 5G

Available as

K-HPA10W-1721	17-20.5 GHz bare die GaN HPA
K-HPA10W-1721-EVAL	17-20.5 GHz bare die GaN HPA evaluation board
K-HPA10W-1721-SM	17-20.5 GHz packaged GaN HPA
K-HPA10W-1721-SM-EVAL	17-20.5 GHz packaged GaN HPA evaluation board
K-HPA10W-1721-SSPA	17-20.5 GHz GaN solid state power amplifier

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Electrical Specification

Freq 17-20.5 GHz, $T_a=25\text{ }^\circ\text{C}$ $V_d=25\text{ V}$, $I_{dq}=300\text{ mA}$, $Z_o=50\text{ }\Omega$

Parameter	Test Conditions	Min	Typ	High	Unit
Operational Frequency Range		17.0		20.5	(GHz)
Small Signal Gain	17-19 GHz		25		(dB)
	19-20.5 GHz		22		(dB)
Input Return Loss	17.5-20.5 GHz		10		(dB)
Output Return Loss	17.5-20.5 GHz		10		(dB)
Output Power at Saturation	17.5-19.5 GHz		42		(dBm)
	19.5-20.5 GHz		40		(dBm)
Power Added Efficiency	Pin=20 dBm		33		(%)
	17.5-19 GHz		25		(%)
	19-20 GHz		20		(%)
	20.5 GHz		20		(%)
Output Power Temperature Coefficient	19 GHz, P_{sat} -40 to 85 $^\circ\text{C}$		0.03		(dB/ $^\circ\text{C}$)

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_d)	30 V
Gate Voltage Range (V_g)	-8 to 0 V
Drain Current (I_d)	2.5 A
Power Dissipation (PDISS) 85 $^\circ\text{C}$	44 W
Input Power (Pin)	23 dBm
Mounting Temperature (30 seconds)	260 $^\circ\text{C}$
Storage Temperature	-55 to 150 $^\circ\text{C}$
Junction Temperature	200 $^\circ\text{C}$

Exceeding any one or combination of these limits may cause permanent damage to this device. Sustained operation near these survivability limits is not recommended.

Recommended Operating Conditions

Parameter	Rating
Drain Voltage (V_d)	20-30 V
Gate Voltage Range (V_g)	-3.6 (TYP)
Drain Current, Quiescent (I_{dq})	300 mA
Junction Temperature	<200 $^\circ\text{C}$

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Thermal Reliability Information

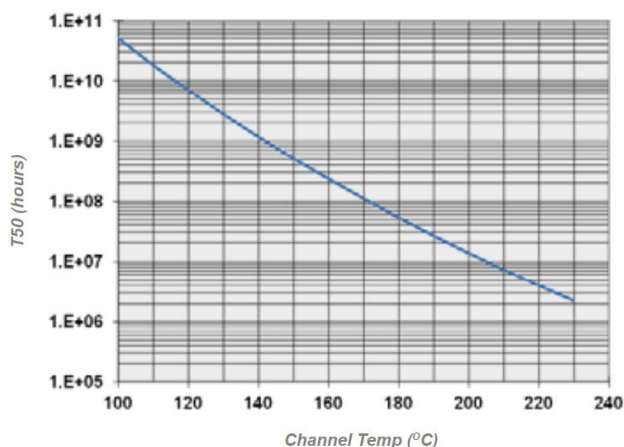
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{jc}) ⁽¹⁾	T _{base} = 85 °C, V _d =25 V, I _d =0-1.5 A	2.62	°C/W

Notes:

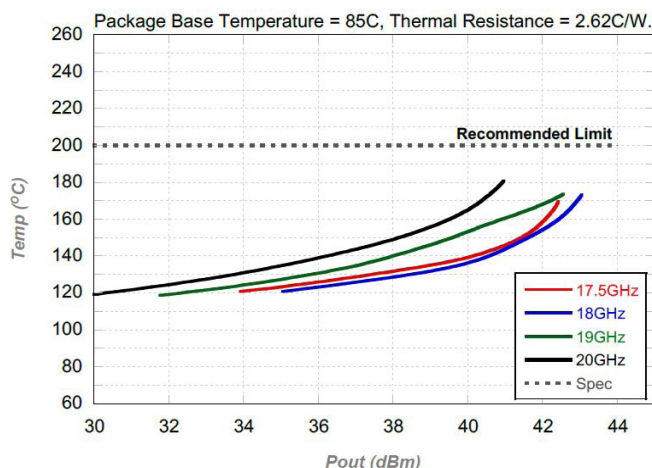
Thermal resistance measured using Raman Thermography on device channel referenced to back of package.

Median Time To Failure vs Channel Temperature

0.25 um GaN process

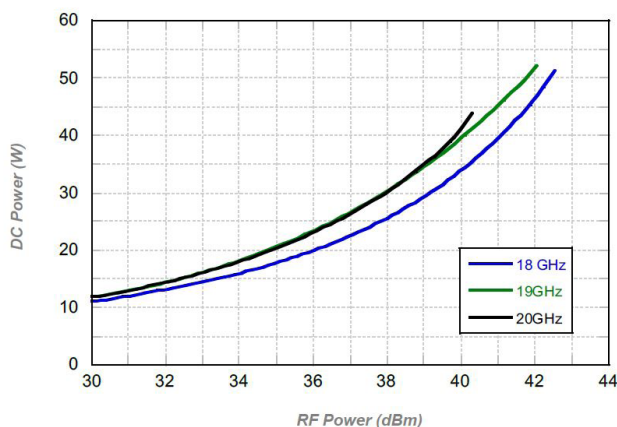


Channel Temperature vs Pout



Power Consumption

DC power consumption vs output power



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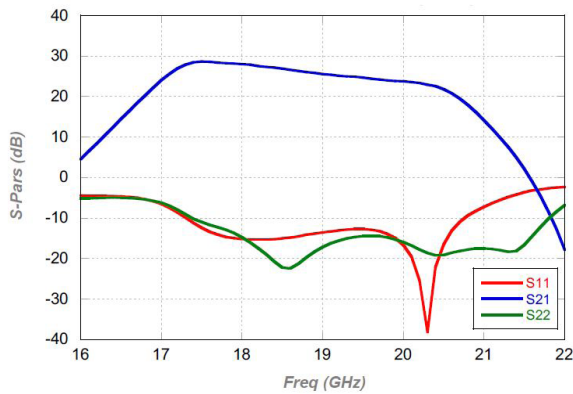


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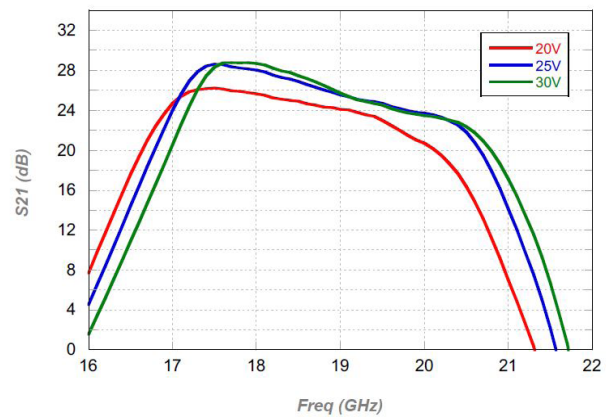
Small Signal Performance Curves

$V_D=25\text{ V}$, $I_{DQ}=300\text{ mA}$, $V_G\sim-3.6\text{ V}$ typical, $T_A=25\text{ }^\circ\text{C}$

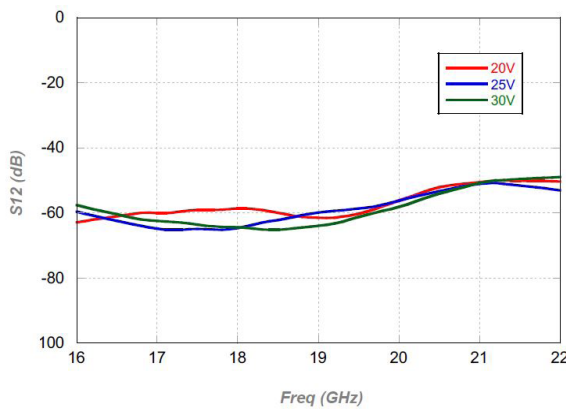
S-Parameters vs Frequency



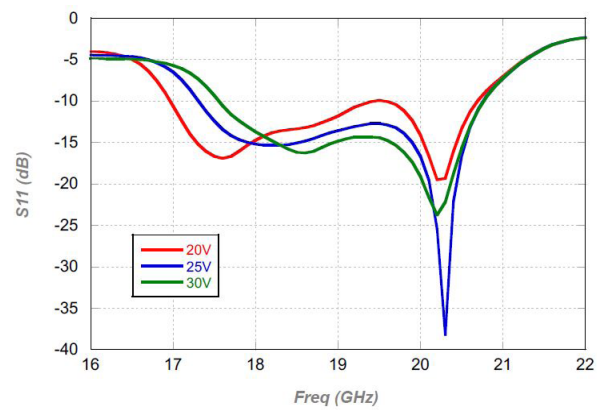
Small Signal Gain vs Frequency vs Drain Voltage



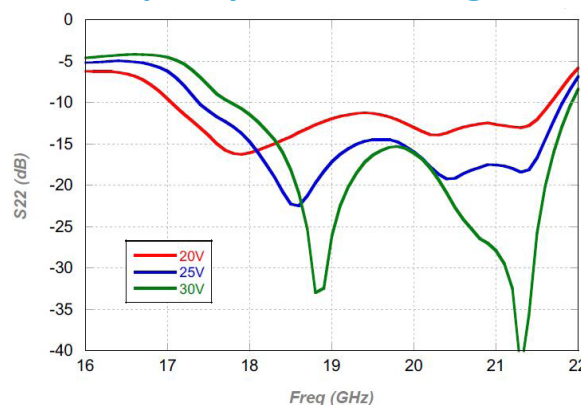
Reverse Gain vs Frequency vs Drain Voltage



Input Return Loss vs Frequency vs Drain Voltage



Output Return Loss vs Frequency vs Drain Voltage



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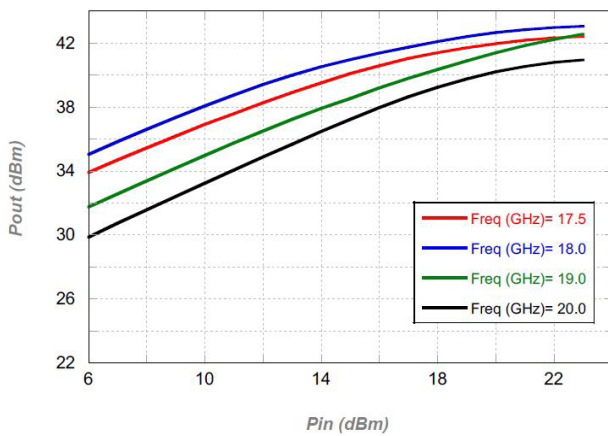


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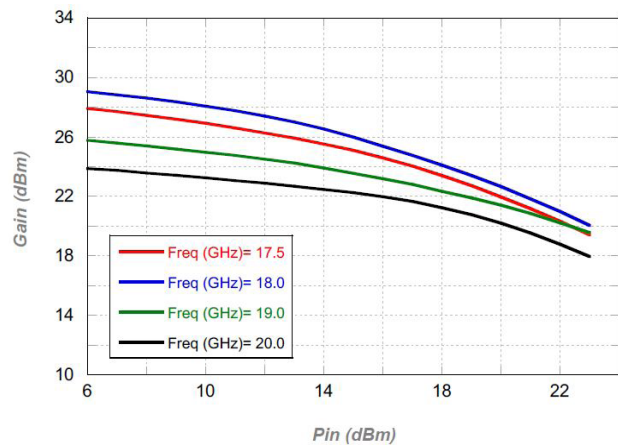
Large Signal Performance Curves

$V_D=25\text{ V}$, $I_{DQ}=300\text{ mA}$, $V_G\sim-3.6\text{ V}$ typical, $T_A=25\text{ }^\circ\text{C}$

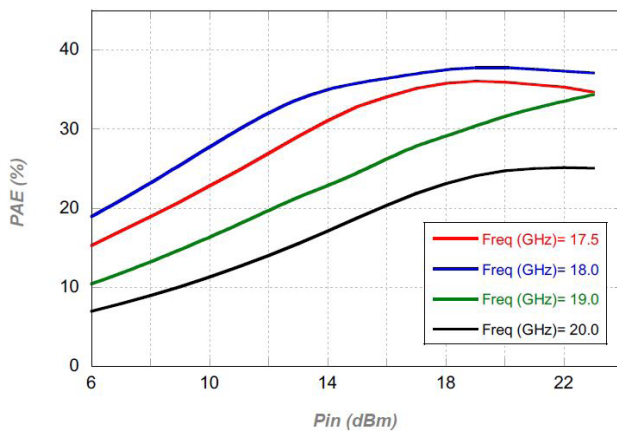
Pout vs Pin vs Frequency



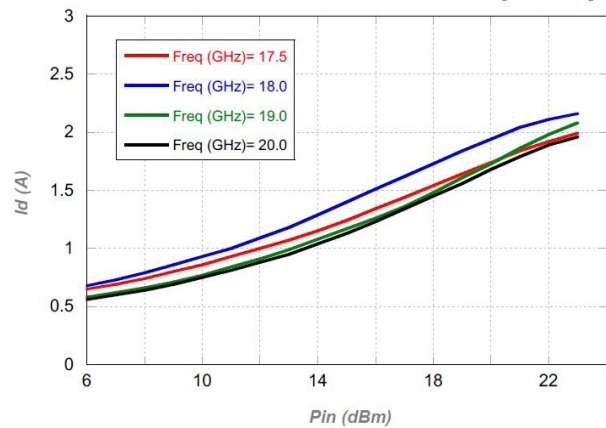
Gain vs Pin vs Frequency



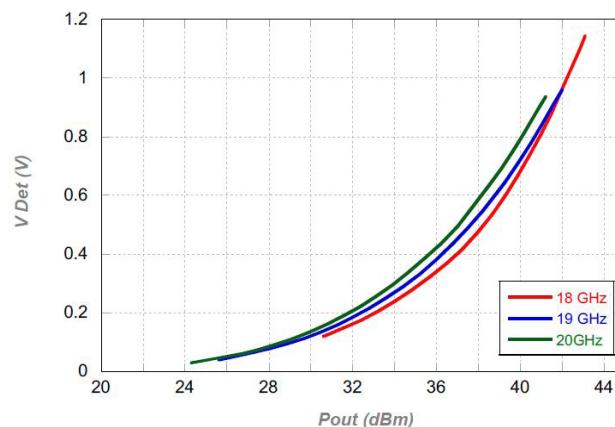
PAE vs Pin vs Frequency



Drain Current vs Pin vs Frequency



Power Detect Voltage vs Pout



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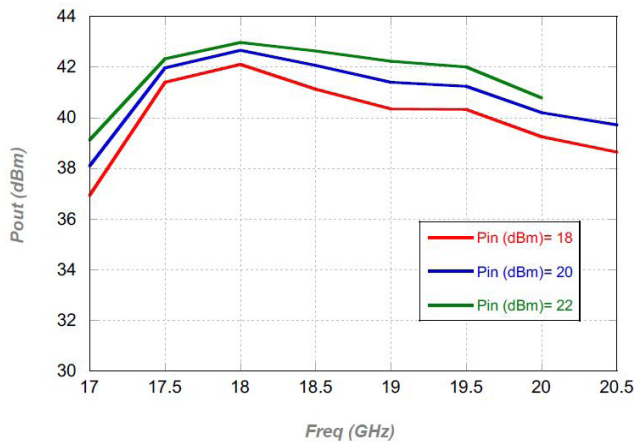


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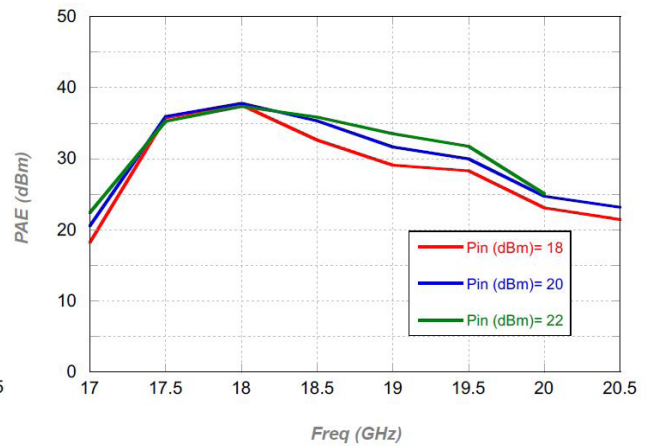
Large Signal Performance Curves

$V_D=25\text{ V}$, $I_{DQ}=300\text{ mA}$, $V_G\sim-3.6\text{ V}$ typical, $T_A=25\text{ }^\circ\text{C}$

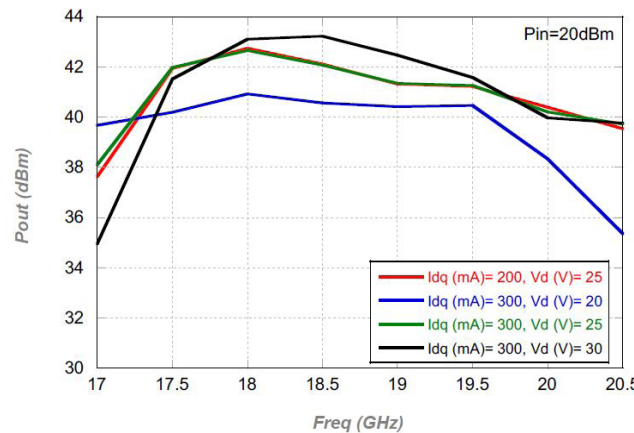
Pout vs Frequency vs Pin



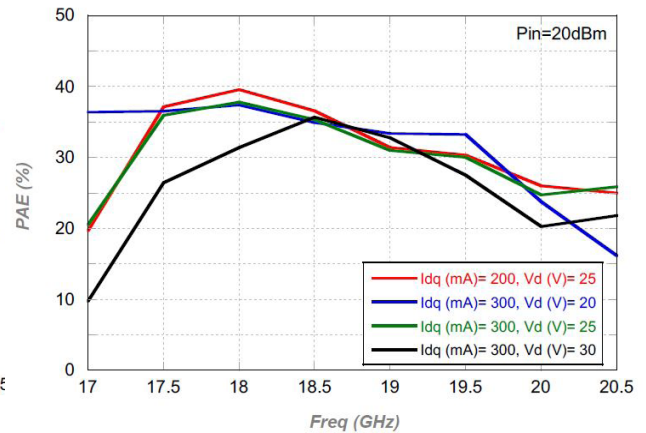
PAE vs Frequency vs Pin



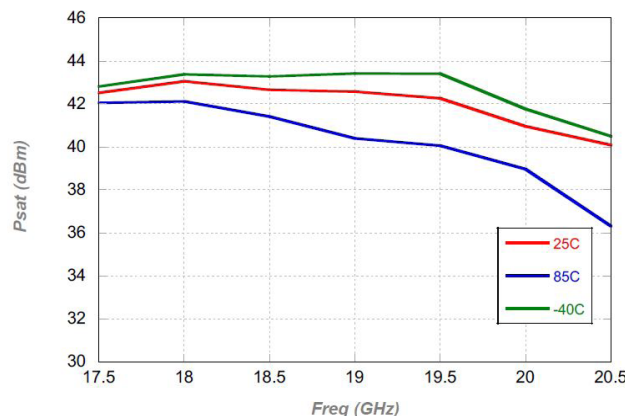
Pout vs Frequency vs Bias



PAE vs Frequency vs Bias



Saturated Power vs Frequency vs Temperature



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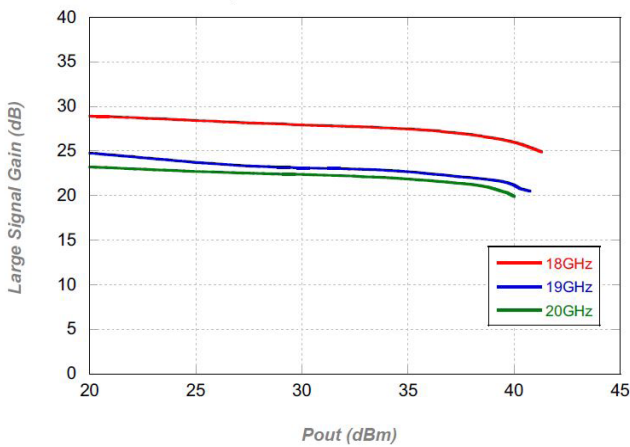


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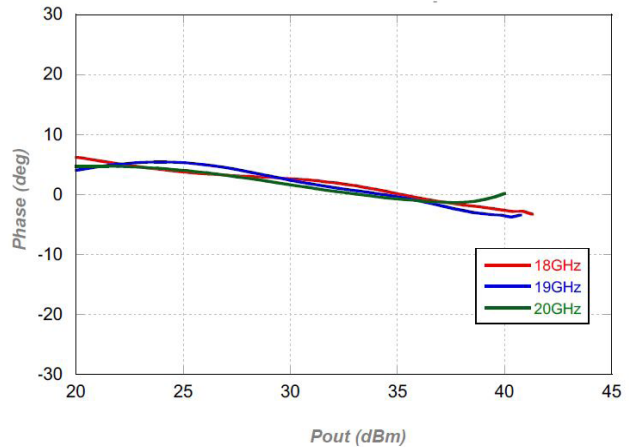
Linearity Performance Curves

$V_D=25\text{ V}$, $I_{DQ}=300\text{ mA}$, $V_G\sim-3.6\text{ V}$ typical, $T_A=25\text{ }^\circ\text{C}$

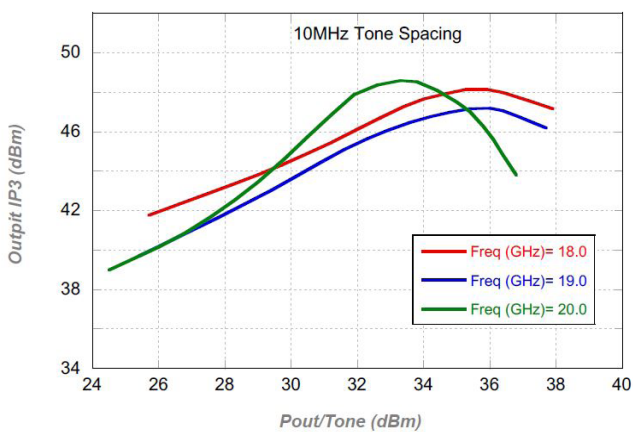
AM/AM vs Frequency



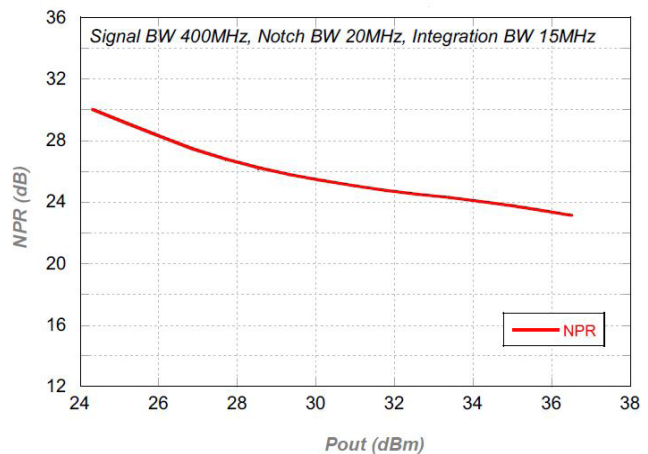
AM/PM vs Frequency



Output IP3 vs Pout/Tone vs Frequency



Noise Power Ratio vs Average Pout at 19 GHz



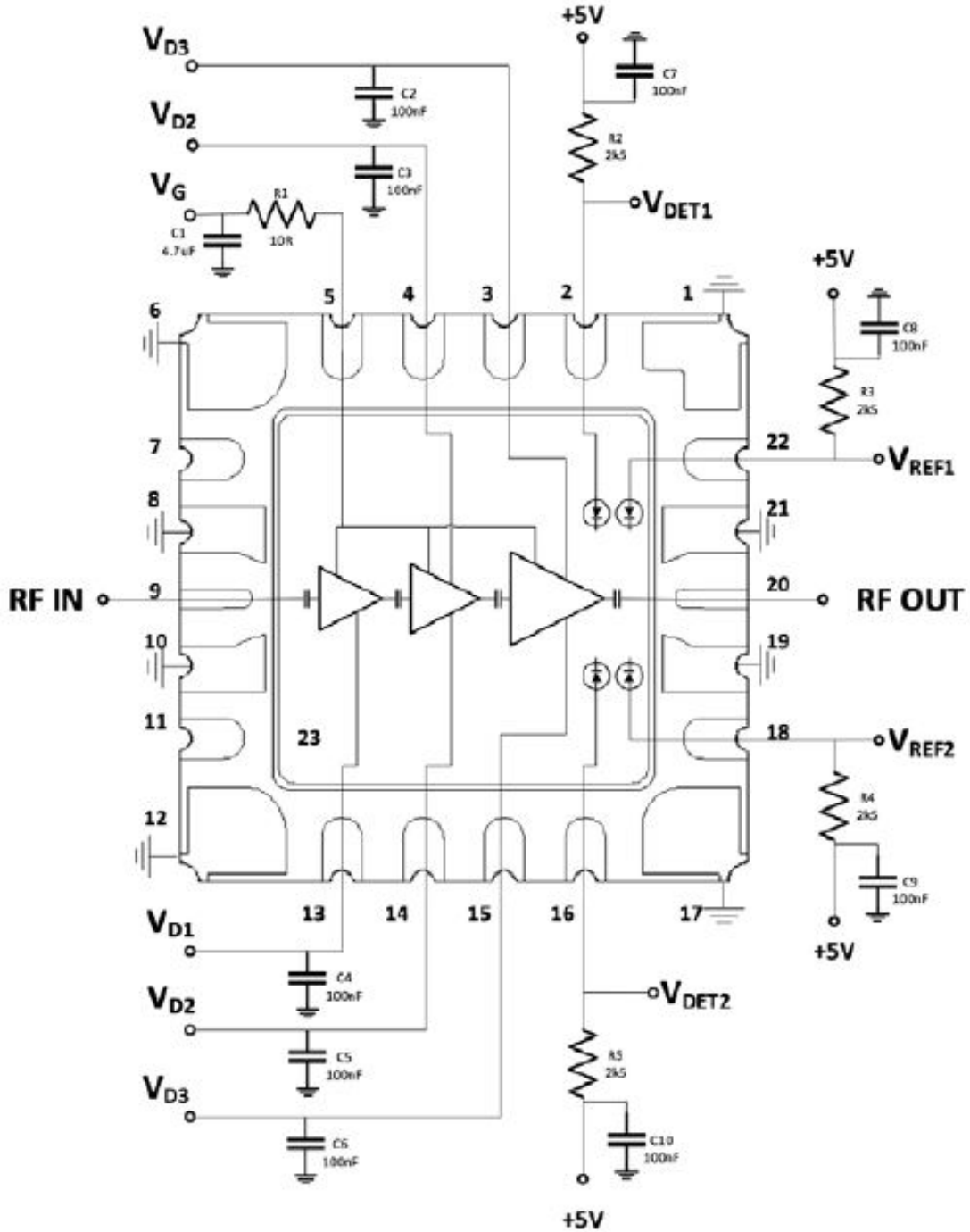
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Recommended Application Circuit



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Bill Of Materials

Part	Vale	Case Size
C1	4.7 μ F	1608 (0603)
C2, C3, C4, C5. C6. C7, C8, C9 C10	100 nF	1608 (0603)
R1	10 Ohm	1005 (0402)
R2, R3, R4, R5	2.5k Ohm	1005 (0402)

Bias Sequences

Bias Up Sequence	Bias Down Sequence
1. Set ID limit to 2.5 A, IG limit to 50 mA	1. Turn off RF supply
2. Apply -5 V to VG	2. Reduce VG to -5 V
3. Apply +25 V to VD; IDQ is \sim 0 mA	3. Set VD to 0 V
4. Adjust VG until IDQ = 300 mA (VG \sim -3.6 V)	4. Turn off VD supply
5. Turn on RF supply	5. Turn off VG supply

Arrangement

D2 and D3 must be biased from both sides.

Drain side capacitors should be 35 V minimum rating.

Bypass capacitors should be placed as close to the packaged device as possible.

Detector Operation

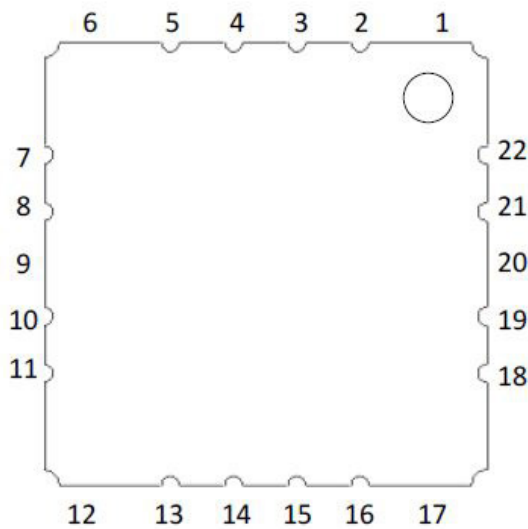
K-HPA10W-1721-SM includes power detectors on both sides of the device to facilitate integration into larger systems. The power detector requires an external 5V supply. For temperature compensation, the VDET and VREF outputs can be connected to a voltage comparator circuit, the output from which can be fed into an ADC or multimeter for the result.

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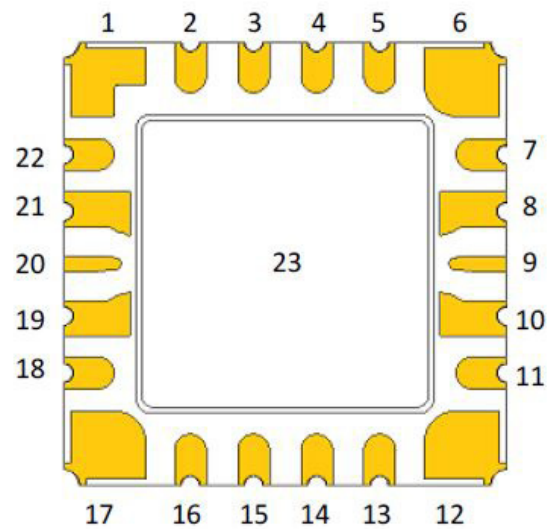


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Pin Descriptions



Top View



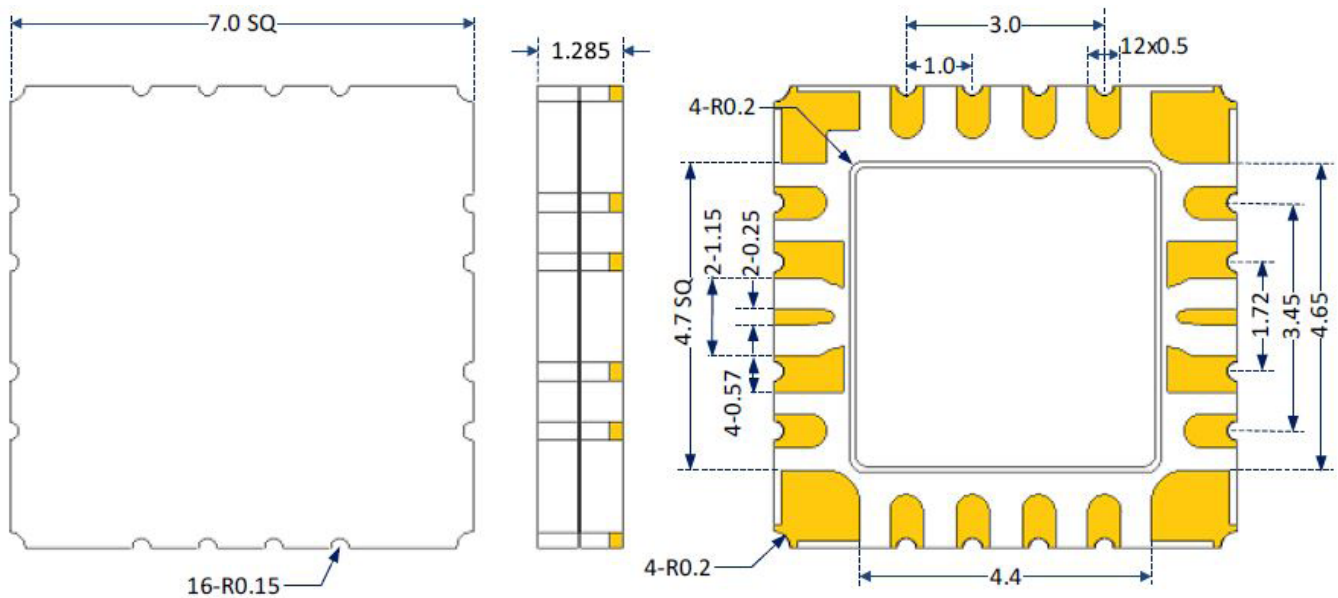
Bottom View

Pad Number	Label	Description
1, 6, 8, 10, 12, 17, 19, 21, 23	GND	Ground
2, 16	V _{DET}	Detector Diode Output Voltage
3, 15	V _{D3}	Drain Voltage Stage 3
4, 14	V _{D2}	Drain Voltage Stage 2
5	V _G	Gate Voltage (all stages)
7, 11	NC	No Connect
9	RF _{IN}	RF Input, 50 Ω matched, DC Blocked
13	V _{D1}	Drain Voltage Stage 1
18, 22	V _{REF}	Reference Diode Output Voltage
20	RF _{OUT}	RF Output, 50 Ω matched, DC Blocked

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Units: mm
Tolerances ± 0.15

Materials:
Package: Metal/Ceramic
Lid: Metal/Ceramic

Melted Au-Sn preform is bonded on the plated surface
Metal Finish: Ni PLATE + Au PLATE 1.0 μ MIN.

Marking:
ARRALIS: Company Logo
LE-K1330308-SM: Product Code
YYWW: Date Code
XXX-XXX-XXX: Lot Number

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General Notes On Assembly

1. Clean the board or module with alcohol and allow it to fully dry.
2. Apply solder paste to each pin and heat achieve re-flow, being careful not to exceed the thermal budget.
3. After completing the soldering process, allow the devices to cool naturally for at least 3 minutes.
4. Avoid any mechanical stress or shock to the solder joints and devices during cooling,
5. Clean the assembly with alcohol.

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C

Handling Precautions

Parameter	Rating
ESD - Human Bodel Model (HBM)	TBD



CAUTION!
ESD – Sensitive Device

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Application Notes

It is typical for GaN HPAs to exhibit a soft compression characteristic as can be seen on the AM/AM plot. This can have a detrimental impact on some modulation schemes particularly where a high PAPR is used. Modern digital techniques such as Digital Pre-Distortion (DPD) can be applied to an input signal to linearize the performance and achieve significant improvements on the EVM. By applying DPD to K-HPA10W-1721-SM it is possible to linearize the HPA. The subsequent graphs of AM/AM and AM/PM show linear performance beyond 40dBm output power. The measurement uses Direct DPD over a signal bandwidth of 400 MHz and 10 dB PAPR.

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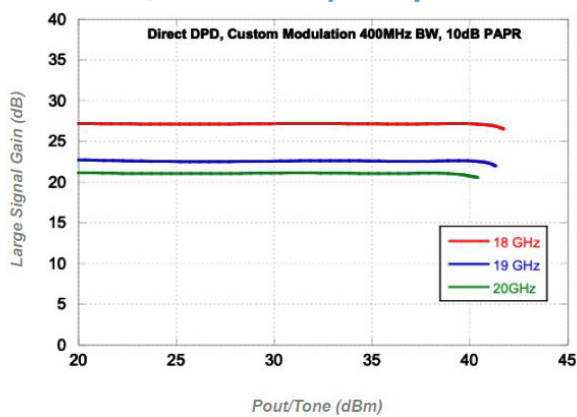


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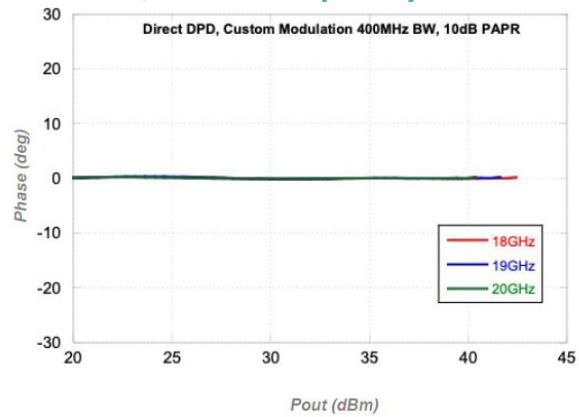
DPD Implementation Process Curves

$V_d=25$ V, $I_{DQ}=300$ mA, $V_G\sim 3.6$ V typical, $T_A=25$ °C

AM/AM vs Frequency



AM/PM vs Frequency



Frequency	18	19	20	GHz
Signal Bandwidth	400	400	400	MHz
EVM	1.6	1.6	0.9	%
Pin (avg)	5.2	8.8	8.8	dBm
Pout (avg)	33.6	32.4	31	dBm
Pout (max)	42.1	42.0	40.6	dBm
Gain	28.4	23.6	22.2	dB
Crest Factor	10	10	10	dB

Contact Information

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