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T4R4_060_096

60-GHz Highly Integrated MIMO Transceiver with four Receivers and four Transmitters

Preliminary Data Sheet

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Version Control

Version	Changed section	Description of change	Reason for change
0.1	(all)	Creation of initial version of document	
0.2	(all)	Adaptation of section “Specification”	Provision of a preliminary document
0.3	(all)	Minor corrections in layout	Release of 1st preliminary document
0.4	(all)	Revision of document	Conversion and update to product version 096

Table of Contents

1 Features

- Radar transceiver for the frequency band at 60 GHz
- Band width of 7 GHz covering 57 to 64 GHz
- Four switchable transmit and four switchable receive channels
- MIMO chip cascade via 20-GHz LO input / output possible
- Single supply voltage of 3.3 V
- Current consumption in TDM operation ≤ 500 mA
- Fully ESD protected device
- Integrated low phase noise VCO
- Transmitter with power control
- Receiver with homodyne quadrature mixer
- Single-ended TX outputs and RX inputs
- LGA121 leadless package 8 × 8 mm²
- Pb-free, RoHS compliant package

1.1 Overview

The T4R4 IC is a highly integrated MIMO transceiver for the 60-GHz ISM band operating and with the target frequency range of < 57 GHz up to > 64 GHz. It includes four transmit and four receive switchable channels to enable time-division-multiplexing operations. The IC is also suitable for massive MIMO chaining with its master / slave mode to boost the achievable angular resolution through 20-GHz LO input / output pads. The output power of the transmitter can be controlled. The internal 20-GHz VCO has an integrated frequency divider with a frequency range of 4.75 GHz – 5.58 GHz. The IC is fabricated in a SiGe BiCMOS technology of IHP GmbH.

1.2 Applications

The 60-GHz MIMO transceiver can be employed in FMCW radars requiring high range resolution thanks to its wide operation bandwidth which is compliant with the frequency band (57 GHz – 64 GHz) opened for industrial radar[1]. Its high operating frequency and high output power enable measurements with improved range accuracy and high detection range. This Radar Transceiver comprises four transmit and receiver channels to enable a full 3+1D resolution of the measurement object and space investigated.

[1] Regulation on frequency range and application scope varies between world regions.

2 Block Diagram

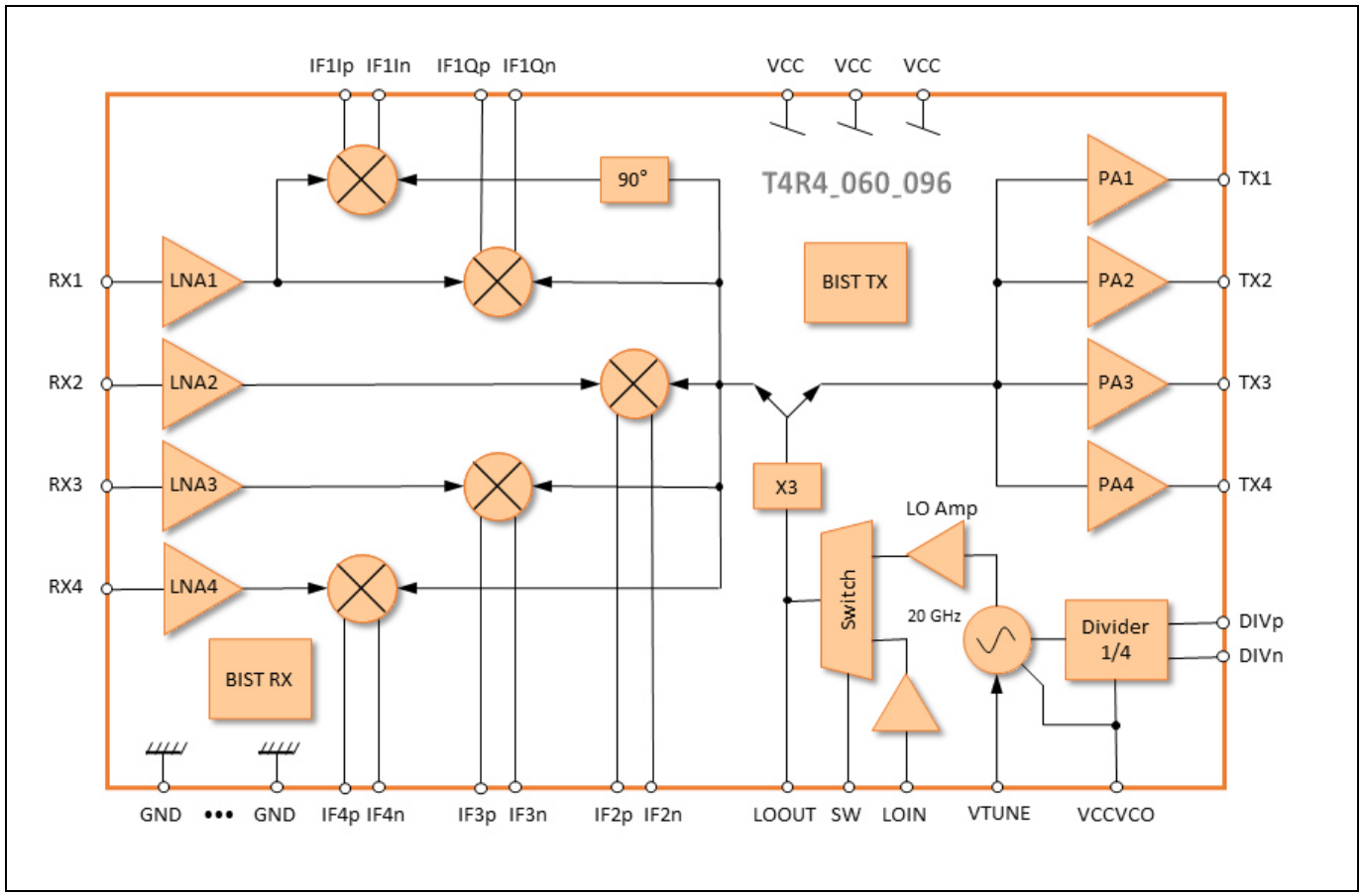


Figure 1 Simplified Block Diagram

3 Land Assignment

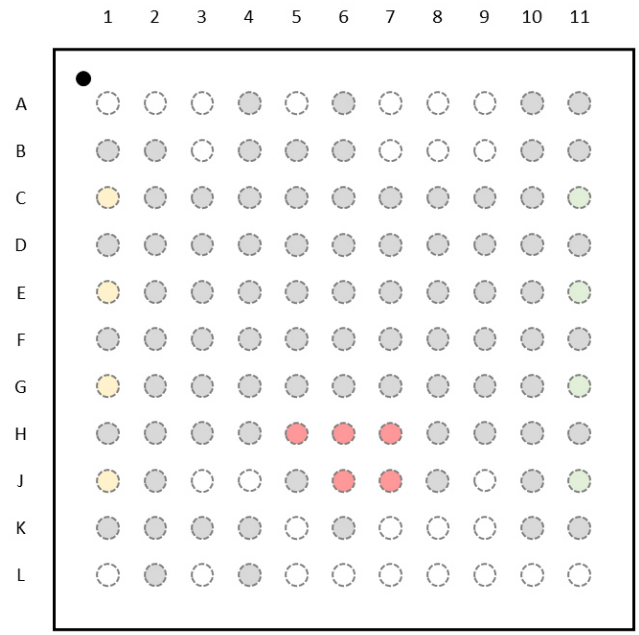


Figure 2 Land Assignment (top view)

Table 1 Land (terminal) description

Location	**Name**	Type	Description
A 1	TXEN1	digital	PA1 enable, 100-kΩ pull-down resistor at input. By default PA1 is off: 0 – off, 3.3 V - enable
A 2	TXEN2	digital	PA2 enable, 100-kΩ pull-down resistor at input. By default PA2 is off: 0 – off, 3.3 V - enable
A 3	TXEN4	digital	PA4 enable, 100-kΩ pull-down resistor at input. By default PA4 is off: 0 – off, 3.3 V - enable
A 4	GND		Ground
A 5	LOOUT	analog	20-GHz LO output, single-ended 50-Ω output (before the frequency tripler), low-ohmic DC path to ground.
A 6	GND		Ground
A 7	IF2n	analog	Negative output of differential RX2-channel outputs, DC coupled, 500-Ω differential termination is recommended.
A 8	IF1Qn	analog	Negative output of differential RX1-channel quadrature outputs, DC coupled, 500-Ω differential termination is recommended.
A 9	IF1In	analog	Negative output of differential RX1-channel in-phase outputs, DC coupled, 500-Ω differential termination is recommended.
A 10, 11	GND		Ground
B 1,2	GND		Ground
B 3	TXEN3	digital	PA3 enable, 100-kΩ pull-down resistor at input. By default PA3 is off: 0 – off, 3.3 V - enable
B 4 - 6	GND		Ground
B 7	IF2p	analog	Positive output of differential RX2 channel outputs, DC coupled, 500-Ω differential termination is recommended.

B 8	IF1Qp	analog	Positive output of differential RX1 channel quadrature outputs, DC coupled, 500-Ω differential termination is recommended.
B 9	IF1Ip	analog	Positive output of differential RX1 channel in-phase outputs, DC coupled, 500-Ω differential termination is recommended.
B 10, 11	GND		Ground
C 1	TX1	analog	TX1 channel antenna, single-ended 50-Ω output
C 2,3	GND		Ground
C 4	LOAMP	digital	PA-on-LOOUT path enable, CMOS Schmitt trigger input, no pull resistor at input. By default PA is off: 0 – off, 3.3 V – enable
C 5-10	GND		Ground
C 11	RX1	analog	RX1 channel antenna, single-ended 50-Ω input
D 1-11	GND		Ground
E 1	TX2	analog	TX2 channel antenna, single-ended 50-Ω output
E 2-10	GND		Ground
E 11	RX2	analog	RX2 channel antenna, single-ended 50-Ω input
F 1-11	GND		Ground
G 1	TX3	analog	TX3 channel antenna, single-ended 50-Ω output
G 2-10	GND		Ground
G 11	RX3	analog	RX3 channel antenna, single-ended 50-Ω input
H 1-4	GND		Ground
H 5-7	VCC	supply	3.3-V supply voltage
H 8-11	GND		Ground
J 1	TX4	analog	TX4 channel antenna, single-ended 50-Ω output
J 2	GND		Ground
J 3	DCOUT	analog	Power-detector output voltage, giving a relative DC voltage with respect to transmitted output power on the TX channel
J 4	TRPEN	digital	Frequency tripler enable, Schmitt trigger input, no pull resistor at input: 0 – tripler is off, 3.3 V – tripler is enabled
J 5	GND		Ground
J 6,7	VCOVCC	supply	3.3-V supply voltage for the VCO
J 8	GND		Ground
J 9	BISTEN	digital	BIST-circuit enable for all receivers, CMOS Schmitt trigger input, no pull resistor at input: 0 – off, 3.3 V – enable
J 10	GND		Ground
J 11	RX4	analog	RX4 channel antenna, single-ended 50-Ω input
K 1-4	GND		Ground
K 5	DIVn	analog	Negative output of differential frequency-divider outputs, $f_{max} \approx 5.5$ GHz, DC coupled
K 6	GND		Ground
K 7	SW	digital	Internal / external LO select input, Schmitt trigger input: 0 V – internal LO from the VCO selected and VCO's supply voltage to be set to 3.3 V 3.3 V – external LO from LOIN input selected and VCO's supply voltage to be set to 0 V
K 8	IF3p	analog	Positive output of differential RX3 channel outputs, DC coupled, 500-Ω differential termination is recommended.
K 9	IF4p	analog	Positive output of differential RX4 channel outputs, DC coupled, 500-Ω differential termination is recommended.
K 10,11	GND		Ground
L 1	TXGAIN	analog	PA gain control voltage, 25-kΩ pull-down resistor at input: 0 – low-power mode, 3.3 V – high-power mode.

			Active gain-setting voltage levels are kept between 1.0 V (lowest output power) and 1.5 V (highest output power).
L 2	GND		Ground
L 3	LOIN	analog	20-GHz external LO input, single-ended 50-Ω input (SW pin set to 3.3 V and VCOVCC to 0 V), low-ohmic DC path to ground.
L 4	GND		Ground
L 5	DIVp	analog	Positive output of differential frequency-divider outputs, f_{max} ≈ 5.5 GHz, DC coupled
L 6	VTUNE	analog	VCO frequency tuning voltage: V_{TUNE} = 0 – 3.3 V
L 7	BISTIN	analog	Input for BIST-circuits of all receivers, requires 100 kHz – 1 MHz sine or square wave test-signal with around 300 mVpp amplitude, DC coupled, voltage divider 200 kΩ / 200 kΩ at input (see 6.4, Input / Output Stages)
L 8	IF3n	analog	Negative output of differential RX3 channel outputs, DC coupled, 500-Ω differential termination with IF3p is recommended.
L 9	IF4n	analog	Negative output of differential RX4 channel outputs, DC coupled, 500-Ω differential termination is recommended.
L 10	TRPGAIN	digital	Frequency tripler gain control voltage, CMOS Schmitt trigger input, no pull resistor at input, by default tripler is operating in the low gain mode: 0 – low gain, 3.3 V – high gain (see 6.4, Input / Output Stages)
L 11	RXEN	digital	Enables all RX channels, CMOS Schmitt trigger input, no pull resistor at input: 0 – all RX channels are off, 3.3 V – all RX channels are enabled

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Supply voltage 1	V_{CC}		3.6	V	to GND
Supply voltage 2	V_{CCVCO}		3.6	V	to GND
DC voltage at RF terminals	V_{DCRF}	0	2	mV	Low-ohmic circuit to ground for TX and RX terminals
DC voltage at tuning input	V_{Vtune}	-0.3	V_{CCVCO} + 0.3	V	
DC voltage at enable/control inputs	V_{EN} / V_{CTL}	-0.3	V_{CC} + 0.3	V	
Input power into RX inputs	P_{IN}		0	dBm	RX1, RX2, RX3, RX4
Junction temperature	T_J	-50	150	°C	
Storage temperature range	T_{STG}		150	°C	
Floor life [2] at factory, ambient (30°C / 60% RH)	FL		168	h	IPC/JEDEC J–STD-033 MSL Level 3 Compliant [1]
ESD robustness	V_{ESD}		*tbd*	V	Human body model, HBM [3]

1) Device storage outside of the packaging is limited according to latest revision of JEDEC Standard IPC/JEDEC J–STD-033. Please follow the handling instructions mentioned there. Further assistance available on request.
2) Allowable time interval after removal from moisture barrier bag, dry storage, dry bake and before solder reflow process.
3) CLASS 1A according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning input	V_{Vtune}	0	V_{CCVCO}	V	
DC voltage at enable inputs	V_{EN}	0	V_{CC}	V	

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R_{thja}			*tbd*	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

T_A = -40°C to +85°C unless otherwise noted, cf. Note 1. Typical values measured at T_A = 25°C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

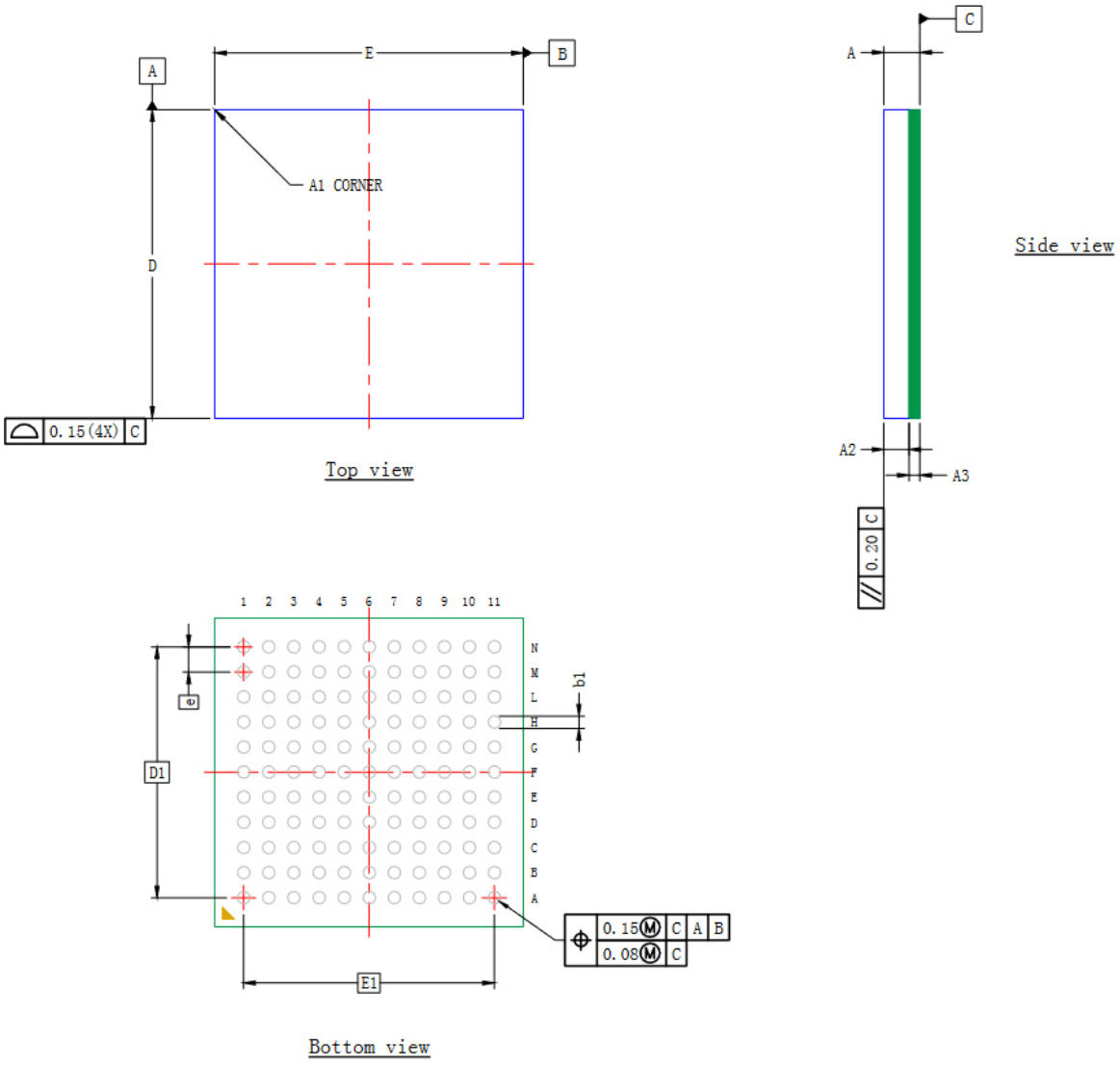
Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
DC Parameters						
Supply current consumption	I_{CC}		420		mA	Enabled all except V(BISTEN) = 0 (BIST off), V(TXGAIN) = 3.3 V (high power)
Enable input voltage, low level	V_{EN_L}	0		0.85	V	
Enable input voltage, high level	V_{EN_H}	2.05		V_{CC}	V	
VCO tuning voltage	V_{Vt}	0		V_{CC}	V	
RF Parameters						
VCO start frequency	f_{TX}		tbd	56.7	GHz	V_{TUNE} = 0
VCO stop frequency	f_{TX}	64.3	tbd		GHz	V_{TUNE} = 3.3 V
VCO tuning full bandwidth	Δf_{TX}	8.6	tbd		GHz	
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		*tbd*		MHz/V	At 60.15 GHz
Transmitter output power	P_{TX}		*tbd*		dBm	Measured 9 dBm at 62 GHz for bare die. Simulated 5 dBm for packaged chip.
Adjustable range output power	P_{TX_adj}		11			V(TXGAIN) = V(TRPGAIN) = 0V min, 3.3V max
Divider ratio of TX signal	N_{div}		12			(4 × 3)
Divider output power	P_{div}		-6		dBm	Note 2
Divider output frequency	f_{div}	4.66		5.53	GHz	(f_{TX} /12)
Divider Phase Noise	P_N	-110	-106		dBc/Hz	At 1 MHz offset at 60.15 GHz
RX conversion gain			*tbd*			Measured 22 dB at 62 GHz for bare die. Simulated 18 dBm for packaged chip.
Adjustable RX conversion gain	G_{RX_adj}					V(TXGAIN) = V(TRPGAIN) =0V min, 3.3 V max
IF frequency range	f_{IF}	0		80	MHz	
IF output impedance	Z_{OUT}		1000		Ω	Differential outputs, simulated
IQ amplitude imbalance	IMB_A		*tbd*		dB	
IQ phase imbalance	IMB_{PH}		*tbd*		deg	
Noise figure (DSB)			10.7		dB	Simulated at 60 GHz
Input compression point	1 dB ICP		*tbd*		dBm	Measured -23dB at 62 GHz for bare die. Simulated -19 dBm for packaged chip.

Note 1: The temperature range and electrical parameters apply to chip operation when only one TX is operational at a time.

Note 2: Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.

5 Packaging

5.1 Outline Dimensions



SYMBOL	Package Dimension					
	Millimeters			Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	0.95	1.00	0.035	0.037	0.039
A2	0.65 REF.			0.026 REF.		
A3	0.282 REF.			0.011 REF.		
b1	0.275	0.325	0.375	0.011	0.013	0.015
D	7.95	8.00	8.05	0.313	0.315	0.317
D1	6.50 BSC			0.256 BSC		
E	7.95	8.00	8.05	0.313	0.315	0.317
E1	6.50 BSC			0.256 BSC		
e	0.65 BSC			0.026 BSC		

NOTES:

1. ALL DIMENSIONS IN MILLIMETER[INCHES]. ANGLES IN DEGREE.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.12[0.005]
3. WARPAGE SHALL NOT EXCEED 0.20[0.008]
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

Figure 3 Land Grid Array Package – LGA121, 8 mm × 8 mm, pitch 0.65 mm

5.2 Package Code

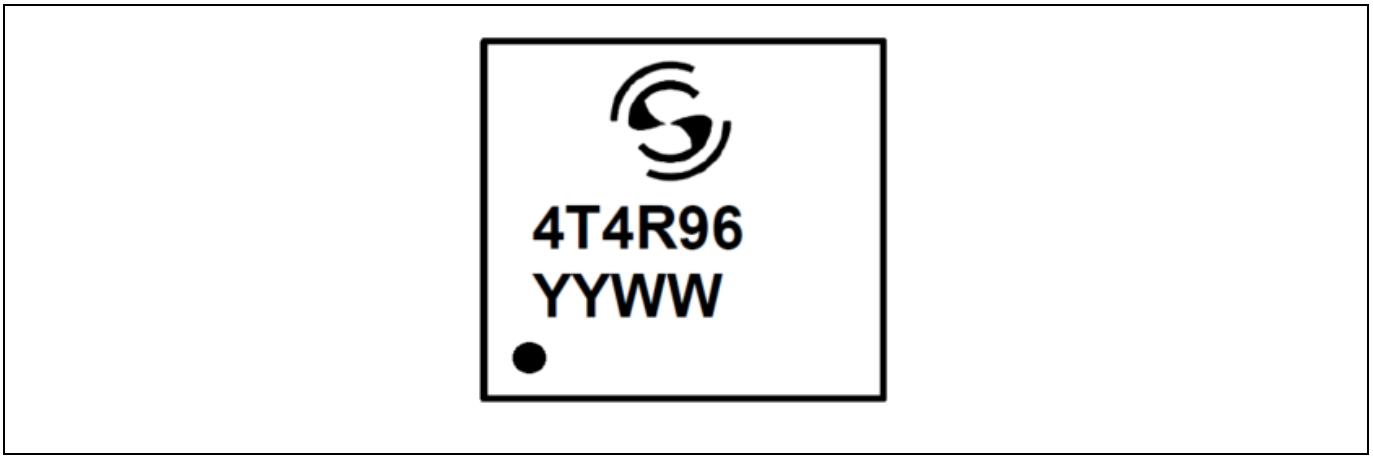


Figure 4 Package Marking

6 Application

6.1 Application Circuit Schematic

[Will be provided at later development stage.]

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Kit

Silicon Radar offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: https://www.siliconradar.com/evalkits/.
The SiRad MIMO r2 platform supports development for of Silicon Radar's integrated IQ transceivers including radar front end boards for T4R4_060_096. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.

Notice:
According to our roadmap the evaluation platform SiRad MIMO r2 shall be extended together with the launch of the T4R4_060_096 transceiver to foster a comprehensive evaluation of this 60 GHz radar chip. However, due to the current supply situation on the world market we are facing a rescheduled launch of the SiRad MIMO r2 for 60 GHz. Thus, shipments will start slightly behind the launch of the radar transceiver chip T4R4_060_096 itself.

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

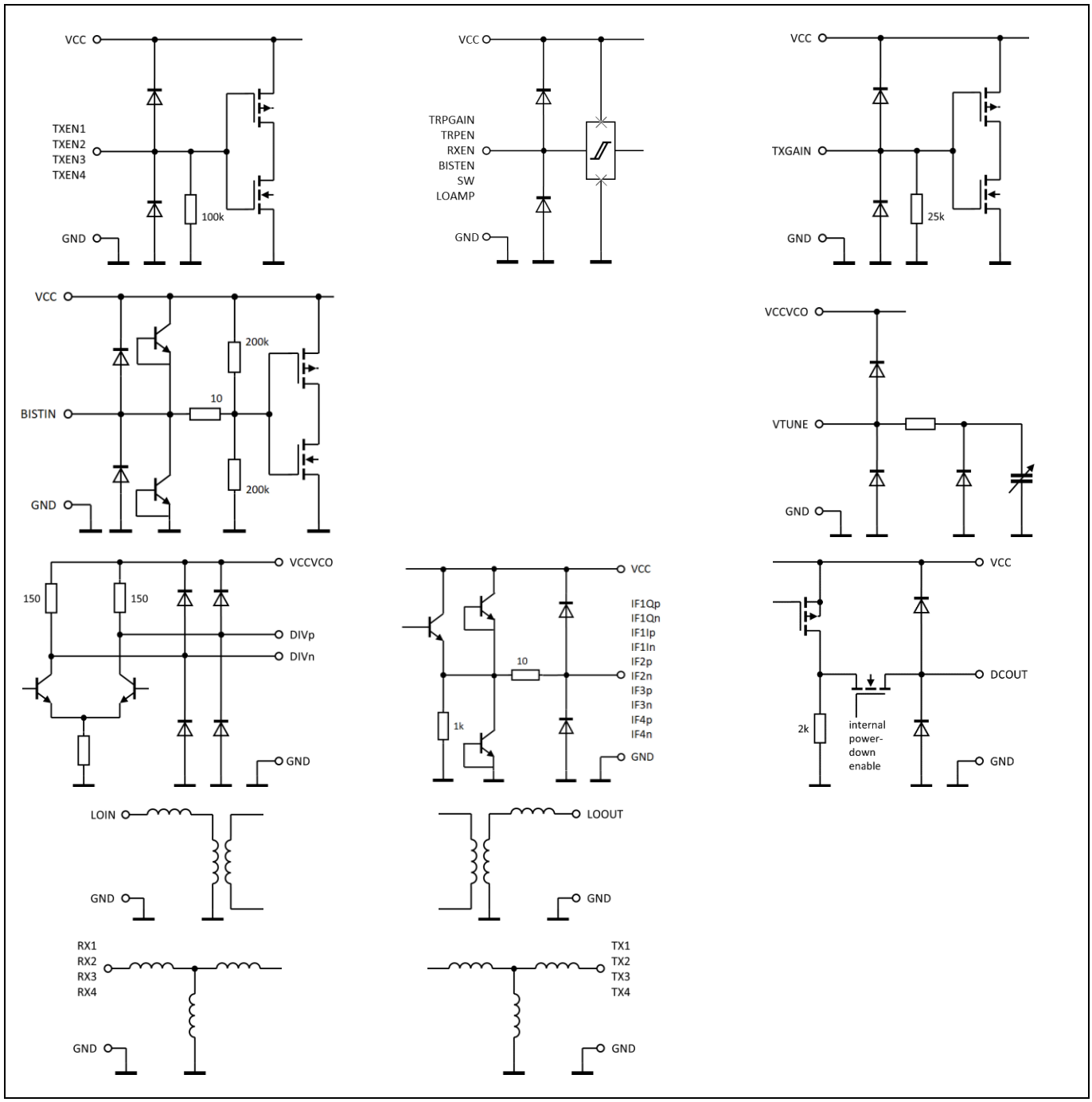


Figure 5 Equivalent I/O Circuits

7 Reliability and Environmental Test

Table 6 Reliability and Environmental Test according to JEDEC Standards

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	tbd
Temperature Cycling	JESD22-A104	850 cycles at -40°C … 125°C	tbd
HTSL	JESD22-A103	1,000 h at 150°C	tbd
HTOL	JESD22-A108	1,000 h at 85°C	tbd
THB	JESD22-A101	1,000 h at 85°C and 85% RH	tbd

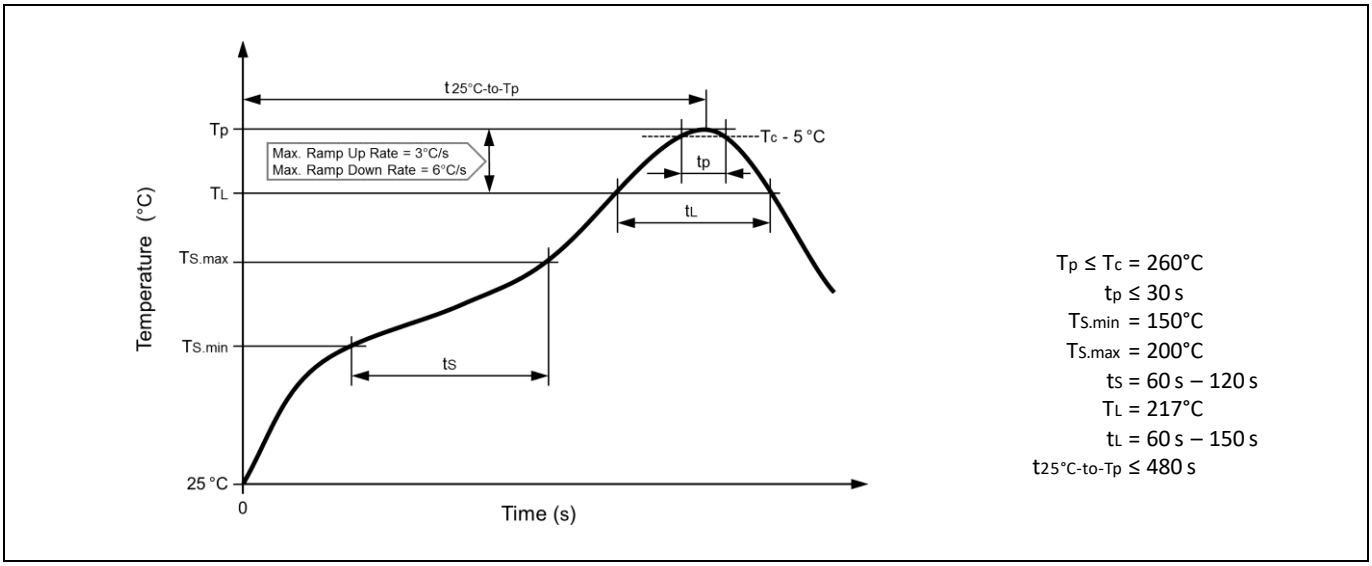


Figure 6 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

8 Measurement Results

Will be provided at later state as test campaigns are completed.

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