SILICON radar

is now

indie SEMICONDUCTOR

indie Semiconductor FFO GmbH

To learn more about indie Semiconductor, please visit our website at www.indiesemi.com

For customer support, please contact us at: dfo.support@indiesemi.com

TR2_060_095

60-GHz Highly Integrated IQ Transceiver with two Receivers

Preliminary Data Sheet

Status:	Date:	Author:	Filename:	
Preliminary	10-July-2023	Indie Semiconductor FFO GmbH	Datasheet_TR2_060_095_V0.3	
Version:	Product number:	Package:	Marking:	Page:
0.3	TR2_060_095	LGA, 6 × 6 mm²	T2R95 YYWW	1 of 15
Document:	Annex to VA_U03_01	Anlage 8_Template_Datenblatt_RevE	Date: 19-May-2020	Rev E

Version Control

Version	Changed section	Description of change	Reason for change
0.1	Template, results	Created with the latest template and updated according to latest results	Update
0.2		Release of document TR2_060_065	
0.3	(all)	Conversion to TR2_060_095	TR2_060_095 datasheet

Table of Contents

1 Features

- Radar transceiver for 60-GHz ISM band
- One transmit and two receive channels
- Single supply voltage of 3.3 V
- Power consumption of 610 mW in continuous operation
- Integrated low phase noise VCO
- Transmitter with power control
- Receiver with homodyne quadrature mixer
- Single-ended TX / RX input / outputs
- LGA64 leadless package 6 × 6 mm²
- Pb-free, RoHS compliant package

1.1 Overview

The TR2 is an integrated transceiver circuit for the 60-GHz ISM band operating in the frequency range of 57 GHz – 64 GHz. It has one transmit and two receive channels. The two receiver channels have a gain-controlled low-noise amplifier (LNA), quadrature mixers, poly-phase filters and one transmitter having a gain-controlled power amplifier (PA) and a voltage-controlled oscillator (VCO) with digital band switching and a divide-by-32 circuit. The output power of the transmitter can be controlled by two digital voltages. The IC is fabricated in a SiGe BiCMOS technology of IHP GmbH.

1.2 Applications

The 60-GHz double-receive channel transceiver can be employed in FMCW radars requiring high range resolution thanks to its wide operation bandwidth which is compliant with the allowed industry & ISM band (57 GHz – 64 GHz). Its high operation frequency and high output power allows measurements with improved range accuracy and maximum detection range. The two receiver channels provide a radar structure where angular resolution is increased, and target angle of arrival measurements can be conducted.

2 Block Diagram

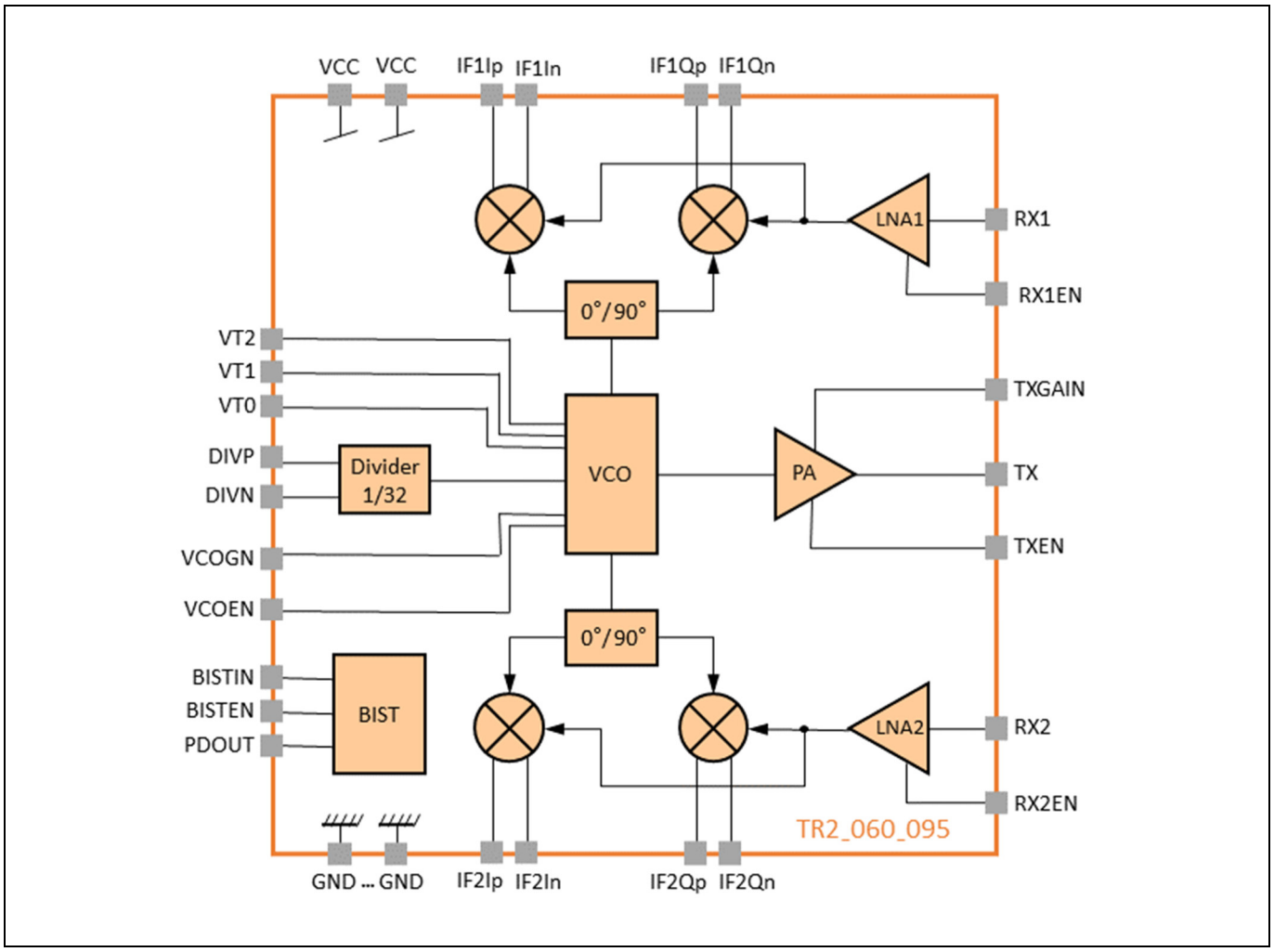


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

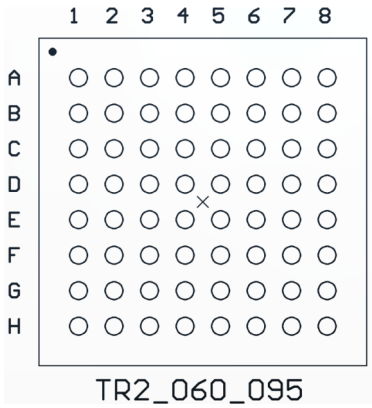


Figure 2 Pin assignment (FCLGA, top view)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
A1	GND	Ground pad
A2	TXEN	PA enable, no pull-up / pull-down resistors. 0 V (PA disable) / 3.3 V (PA enable), ***digital.***
A3	TXGAIN	PA gain control voltage with pull-down resistor of 100 kΩ. By default, PA is set to low output power operation mode: 0V- low power mode, 3.3 V - high power mode; ***analogue***. Active gain setting voltage levels are kept between 1.0 V (lowest output power) – 1.5 V (highest output power).
A4	VCC	Chip supply voltage: 3.3 V
A5	BISTIN	RX channel BIST circuit input signal, requires 100 kHz – 1 MHz test signal having around 300 mVpp amplitude (sine or square wave).
A6	IF1Qn	IF I/Q (In-phase & Quadrature) differential outputs for RX1.
A7	IF1In	
A8	IF1Ip	
B1	PDOUT	Power detector output voltage giving a relative DC voltage with respect to transmitted output power on the TX channel.
B2-B3	GND	Ground pad
B4	VCC	Chip supply voltage: 3.3 V
B5	BISTEN	RX channel BIST circuit enable (input with Schmitt trigger), no pull-up / pull-down resistors. 0 V - disable, 3.3 V - enable; ***digital.***
B6	IF1Qp	IF I/Q (In-phase & Quadrature) differential outputs for RX1.
B7-B8	GND	Ground pad
C1-C8	GND	Ground pad
D1	TX	TX channel antenna single-ended, 50 Ohm output.
D2-D7	GND	Ground pad
D8	RX1	RX1 channel antenna single-ended, 50 Ohm input.
E1-E8	GND	Ground pad
F1	DIVP	Frequency divider differential outputs (1.75GHz – 2.03GHz), DC coupled.
F2-F7	GND	Ground pad

F8	RX2	RX2 channel antenna single-ended, 50 Ohm input.
G1	DIVN	Frequency divider differential outputs (1.75GHz – 2.03GHz), DC coupled.
G2	GND	Ground pad.
G3	VT1	VCO frequency tuning voltages: 0 V – 3.3 V, ***analogue***
G4	VCOGN	VCO gain control voltage (input with Schmitt trigger), no pull-up / pull-down resistors. 0 V - low gain, 3.3 V - high gain; ***digital.***
G5	RX2EN	RX channel 2 enable (input with Schmitt trigger), no pull-up / pull-down resistors. 0 V – disable, 3.3 V – enable; ***digital.***
G6	IF2Qp	IF I/Q (in-phase & quadrature) differential outputs for RX2.
G7-8	GND	Ground pad
H1	VCOEN	VCO enable (input with Schmitt trigger), no pull-up / pull-down resistors. 0 V – disable, 3.3 V – enable; ***digital.***
H2	VT0	VCO frequency tuning voltages: 0 V – 3.3 V, ***analogue***
H3	VT2	
H4	VCC	Chip supply voltage: 3.3 V
H5	RX1EN	RX channel 1 enable (input with Schmitt trigger), no pull-up / pull-down resistors. 0 V – disable, 3.3 V – enable; ***digital.***
H6	IF2Qn	IF I/Q (in-phase & quadrature) differential outputs for RX2.
H7	IF2In	
H8	IF2Ip	

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Supply voltage	V_{CC}		3.6	V	to GND
DC voltage at RF pins	V_{DCRF}	0	2	mV	Low ohmic circuit to GND TX and RX pin; DC coupled DIVout and IF pins
DC voltage at tuning inputs	V_{Vt}	-0.3	V_{CC} + 0.3	V	Inputs VT0, VT1, VT2
DC voltage at enable/control inputs	V_{EN} / V_{CTL}	-0.3	V_{CC} + 0.3	V	
Input power into RX inputs	P_{IN}		0	dBm	RX1, RX2
Junction temperature	T_J	-50	150	°C	
Storage temperature range	T_{STG}		150	°C	
Floor life (out of bag) at factory ambient (30°C / 60% RH)	FL		168	h	IPC/JEDEC J–STD-033A MSL Level 3 Compliant [1)]
ESD robustness	V_{ESD}		tbd	V	Human body model, HBM [2)]

1) Device storage outside of the packaging is limited according to latest revision of JEDEC Standard IPC/JEDEC J–STD-033.
2) CLASS 1A according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011.

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning inputs	V_{Vt}	0	V_{CC}	V	Inputs Vt0 – Vt2
DC voltage at enable inputs	V_{EN}	0	V_{CC}	V	

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R_{thja}			tbd	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

T_A = -40°C to +85°C unless otherwise noted. Typical values measured at T_A = 25°C and V_{CC} = 3.3 V.

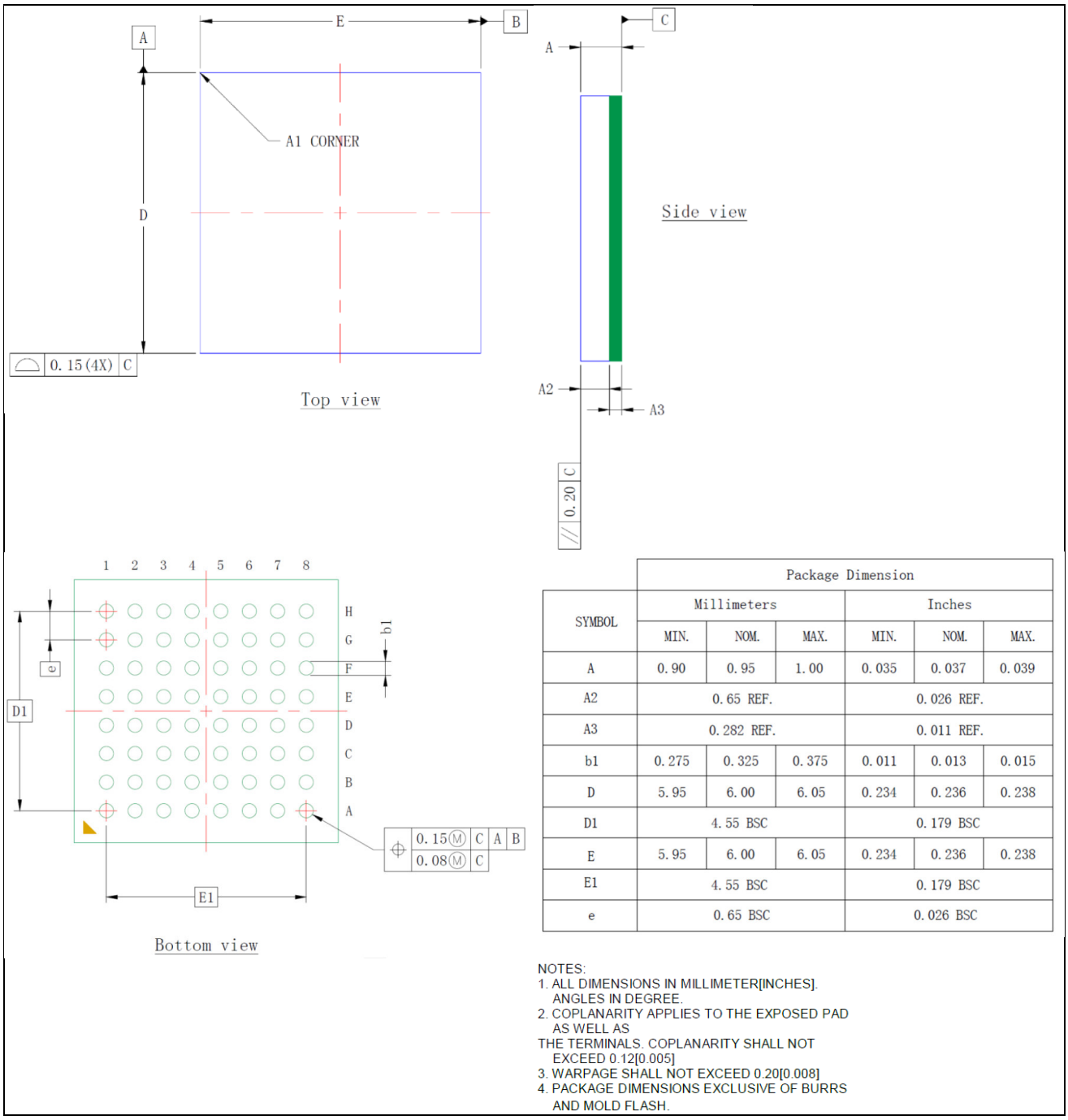
Table 5 Electrical Characteristics (expected values, measurement of first samples pending)

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
DC Parameters						
Supply current consumption	I_{CC}		185		mA	Enabled all, gain max.
Enable input voltage, low level	V_{EN_L}	0		0.85	V	
Enable input voltage, high level	V_{EN_H}	2.05	2.15	V_{CC}	V	
VCO tuning voltage	V_{Vt}	0		V_{CC}	V	Inputs VT0 – VT2
RF Parameters						
VCO start frequency	f_{TX}		tbd	57	GHz	VT0 = VT1 = VT2 = 0
VCO stop frequency	f_{TX}	64	tbd		GHz	VT0 = VT1 = VT2 = 3.3 V
VCO tuning full bandwidth	Δf_{TX}		9.89		GHz	VT0 – VT2 interconnected
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		715		MHz/V	At 59.85 GHz
Transmitter output power	P_{TX}		*tbd*		dBm	Measured 10 dBm at 62 GHz for bare die. Simulated 6 dBm for packaged chip.
Adjustable range output power	P_{TX_adj}	-2		10.5		PAGAIN, VCOGN to be used to adjust
Divider ratio of TX signal	N_{div}		32			
Divider output power	P_{div}		-8		dBm	Note 1
Divider output frequency	f_{div}	1.75		2.08	GHz	(f_{TX} /32)
Divider Phase Noise	P_N	-130	-125		dBc/Hz	At 1 MHz offset
RX conversion gain			*tbd*			Measured 20 dB at 62 GHz for bare die. Simulated 16 dB for packaged chip.
Adjustable RX conversion gain			10	15		TXGAIN, VCOGN to be used to adjust
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		1000		Ω	Differential outputs (emitter follower type; simulated value)
IQ amplitude imbalance			3		dB	
IQ phase imbalance		-10		10	deg	
Noise figure (DSB)			11.6		dB	Simulated at 60 GHz
Input compression point	1 dB ICP		*tbd*		dBm	Measured -20 dBm at 62 GHz for bare die. Simulated -16 dBm for packaged chip.

Note 1: Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.

5 Packaging

5.1 Outline Dimensions



SYMBOL	Package Dimension					
	Millimeters			Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	0.95	1.00	0.035	0.037	0.039
A2		0.65 REF.			0.026 REF.	
A3		0.282 REF.			0.011 REF.	
b1	0.275	0.325	0.375	0.011	0.013	0.015
D	5.95	6.00	6.05	0.234	0.236	0.238
D1		4.55 BSC			0.179 BSC	
E	5.95	6.00	6.05	0.234	0.236	0.238
E1		4.55 BSC			0.179 BSC	
e		0.65 BSC			0.026 BSC	

NOTES:
1. ALL DIMENSIONS IN MILLIMETER[INCHES].
   ANGLES IN DEGREE.
2. COPLANARITY APPLIES TO THE EXPOSED PAD
   AS WELL AS
THE TERMINALS. COPLANARITY SHALL NOT
   EXCEED 0.12[0.005]
3. WARPAGE SHALL NOT EXCEED 0.20[0.008]
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS
   AND MOLD FLASH.

Figure 3 Outline Dimensions of LGA64, 0.65 mm Pitch, 6 mm × 6 mm

5.2 Package Code

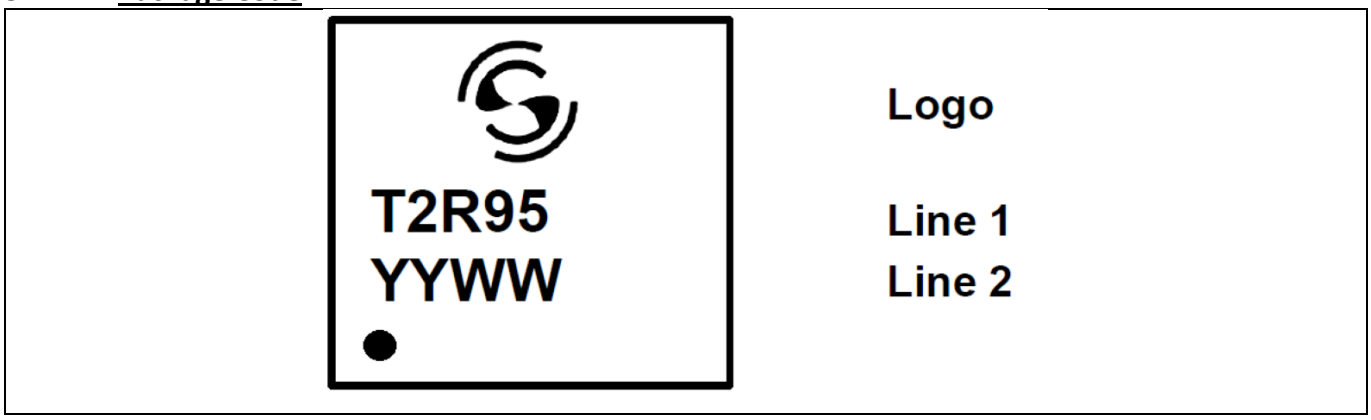


Figure 4 Package Marking as planned, final confirmation pending.

6 Application

6.1 Application Circuit Schematic

Information will be provided on request and at a later stage here.

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Kit

Silicon Radar offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: https://www.siliconradar.com/evalkits/.
The *SiRad Easy® r4* platform supports development for many of Silicon Radar's integrated IQ transceivers including radar front end boards for TR2_060_095. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

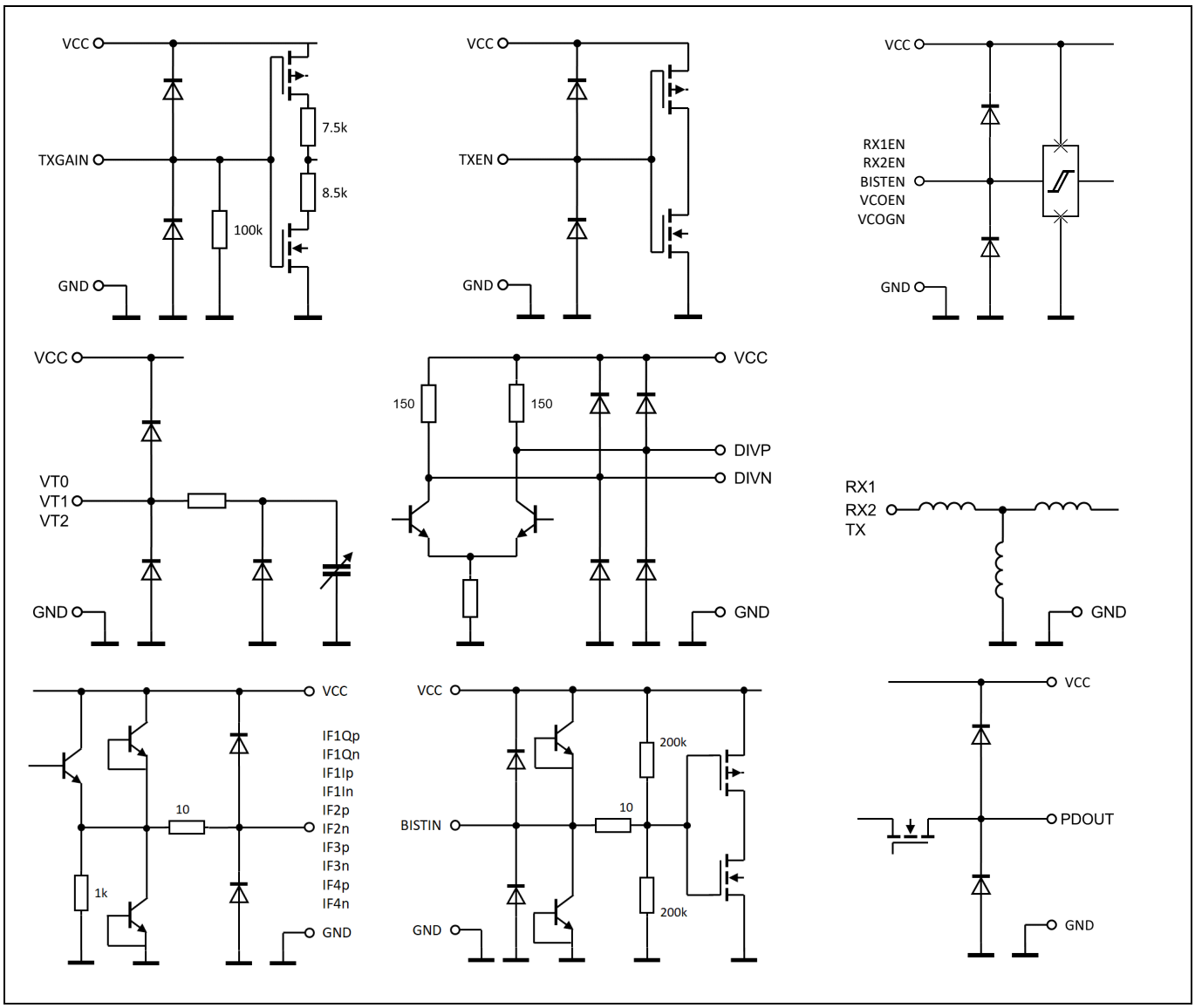


Figure 5 Equivalent I/O Circuits

6.5 VCO Tuning Inputs

The VCO tuning inputs VT0 – VT2 are of analog nature but can be switched digitally as well. The tuning inputs differ in their tuning ranges (tuning bandwidth) and slopes, whereby VT2 has the widest tuning range, and VT0 the narrowest. The VCO tuning range of a specific tuning input can be increased by connecting it to another tuning input. All combinations of the three tuning inputs are allowed. Unused tuning inputs must be set to a fixed potential (between 0 and V_{CC}). The interconnection of all inputs VT0 – VT2 leads to the maximum tuning bandwidth.

7 Reliability and Environmental Test

Table 6 Reliability and Environmental Test according to JEDEC Standards

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	tdb
ELFR	JESD22-A108	Running the burn-in, 48 h at 85°C in 7 runs	tbd
Temperature Cycling	JESD22-A104	850 cycles at -40°C … 125°C	tdb
HTSL	JESD22-A103	1,000 h at 150°C	tdb
HTOL	JESD22-A108	1,000 h at 85°C	tdb
THB	JESD22-A101	1,000 h at 85°C and 85% RH	tdb

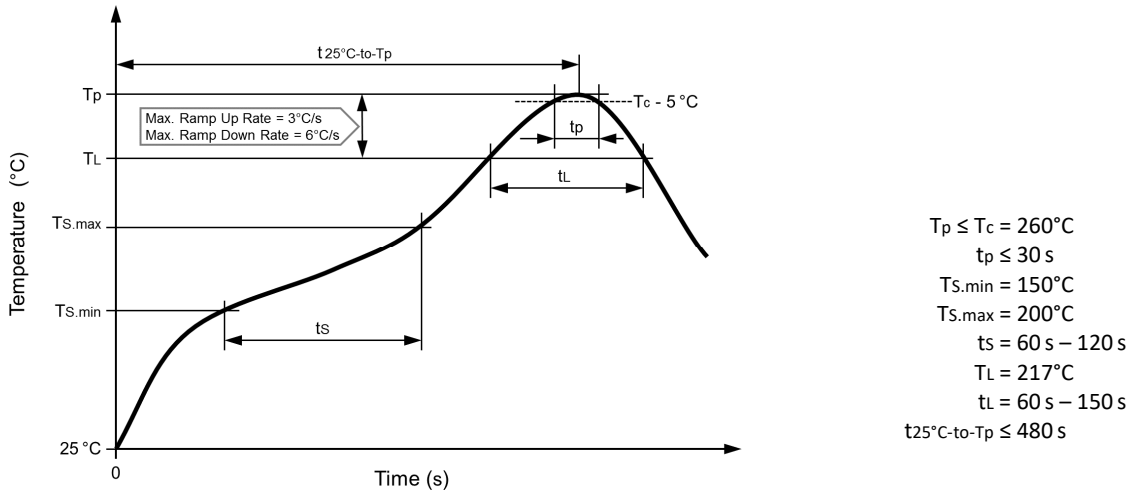


Figure 6 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

Disclaimer

Indie Semiconductor FFO GmbH 2023. The information contained herein is subject to change at any time without notice.
Indie Semiconductor FFO GmbH assumes no responsibility or liability for any loss, damage or defect of a product which is caused in whole or in part by

(i) use of any circuitry other than circuitry embodied in a Indie Semiconductor FFO GmbH product,
(ii) misuse or abuse including static discharge, neglect, or accident,
(iii) unauthorized modifications or repairs which have been soldered or altered during assembly and are not capable of being tested by Indie Semiconductor FFO GmbH under its normal test conditions, or
(iv) improper installation, storage, handling, warehousing, or transportation, or
(v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: Indie Semiconductor FFO GmbH makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any Silicon Radar product and any product documentation. Products sold by Silicon Radar are not suitable or intended to be used in a life support applications or components, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY: BUYER AGREES NOT TO USE INDIE SEMICONDUCTOR FFO GMBH'S PRODUCTS FOR ANY APPLICATIONS OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

Indie Semiconductor FFO GmbH owns all rights, titles and interests to the intellectual property related to Indie Semiconductor FFO GmbH's products, including any software, firmware, copyright, patent, or trademark. The sale of Indie Semiconductor FFO GmbH's products does not convey or imply any license under patent or other rights. Indie Semiconductor FFO GmbH retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by Indie Semiconductor FFO GmbH. Unless otherwise agreed to in writing by Indie Semiconductor FFO GmbH, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.