SILICON radar

is now

indie SEMICONDUCTOR

indie Semiconductor FFO GmbH

To learn more about indie Semiconductor, please visit our website at www.indiesemi.com

For customer support, please contact us at: dfo.support@indiesemi.com

Silicon Radar GmbH
Im Technologiepark 1
15236 Frankfurt (Oder)
Germany

fon +49.335.557 17 74
fax +49.335.557 10 50
https://www.siliconradar.com

TRA_120_002

120-GHz Highly Integrated IQ Transceiver with Antennas on Chip
in Silicon Germanium Technology

Preliminary Data Sheet

Status:	Date:	Author:	Filename:	
Preliminary	2018-11-05	Silicon Radar GmbH	Datasheet_TRA_120_002_V0.8	
Version:	Product number:	Package:	Marking:	Page:
0.8	TRA_120_002	QFN32, 5 × 5 mm²	TRA002 YYWW	1 of 15

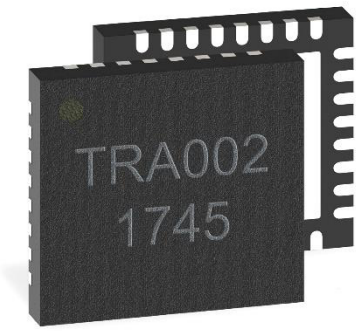
Version Control

Version	Changed section	Description of change	Reason for change
0.5	template	Sections version control and document release added	controlled document
0.6	specification	Spec data revised	routinely revision
0.7	6.5 VCO Tuning Inputs 6.2 Power Cycling 7 Meas. Results	Information parameter and application hint added Application hint added Antenna Radiation Pattern (Fig. 17, 18) added	update update update
0.8	5.4 Qualification Test	Section with reflow profile added	update

Table of Contents

1 Features

- Radar front end (RFE) with on-chip antennas for 122-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 380 mW
  in continuous operating mode
- Integrated low phase noise push-push VCO
- Receiver with homodyne quadrature mixer
- RX and TX dipole on-chip antennas
- Large bandwidth of up to 7 GHz
- QFN32 leadless plastic package 5 × 5 mm²
- Pb-free, RoHS compliant package
- IC is available as bare die as well



1.1 Overview

The radar front end TRA_120_002 is an integrated transceiver circuit for the 122-GHz ISM band with antennas on chip. It includes a low-noise amplifier (LNA), quadrature mixers, a poly-phase filter, a voltage controlled oscillator, divide-by-32 outputs, and transmit and receive antennas (see Figure 1).
The RF signal from the oscillator is directed to the RX path via buffer circuits. The RX signal is amplified by the LNA and converted to baseband by two mixers with quadrature local oscillator (LO). The 120-GHz LO has four analog tuning inputs with different tuning ranges and tuning slopes. The tuning inputs can be combined to obtain a wide frequency tuning range. The analog tuning inputs together with the integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing analog tuning inputs.
The IC is fabricated in SG13S SiGe BiCMOS technology of IHP GmbH.

1.2 Applications

The main field of application for the 120-GHz transceiver radar frontend (RFE) is in short range radar systems with a range up to about 10 meters. By using dielectric lenses, the range can be increased considerably. The RFE can be used in FMCW mode as well as in CW mode. Although the chip is intended for use in the ISM band 122 GHz - 123 GHz, it is also possible to extend the bandwidth to the full tuning range of 7 GHz.

2 Block Diagram

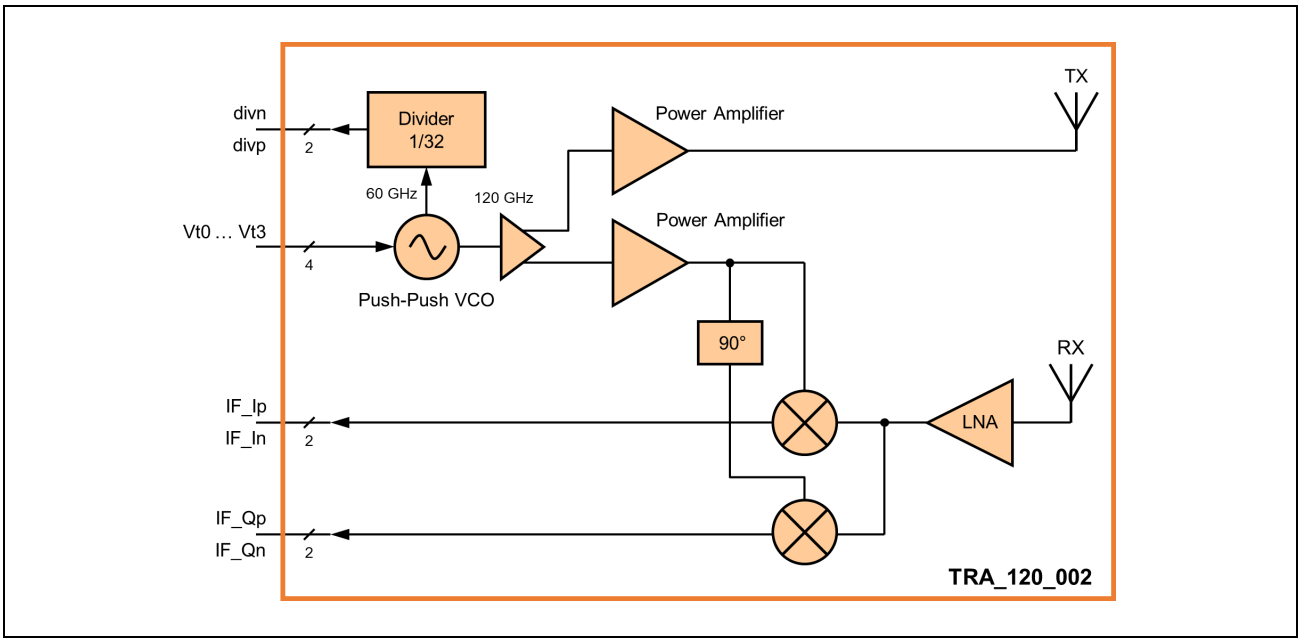


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

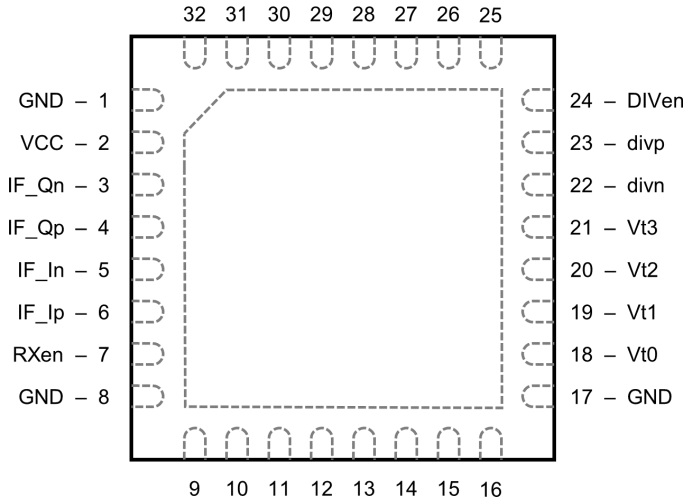


Figure 2 Pin Assignment (QFN32, top view)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
2	VCC	Supply voltage (3.3 V)
3	IF_Qn	Quadrature IF I output, negative terminal (DC coupled)
4	IF_Qp	Quadrature IF I output, positive terminal (DC coupled)
5	IF_In	Quadrature IF Q output, negative terminal (DC coupled)
6	IF_Ip	Quadrature IF Q output, positive terminal (DC coupled)
7	RXen	Receiver enable input, low-active CMOS input with internal 70-kΩ pull-down resistor
18	Vt0	VCO tuning input 0 (0 – V_{CC})
19	Vt1	VCO tuning input 1 (0 – V_{CC})
20	Vt2	VCO tuning input 2 (0 – V_{CC})
21	Vt3	VCO tuning input 3 (0 – V_{CC})
22	divn	Divider output, neg. terminal. 50 Ω, DC coupled, external decoupling cap. required
23	divp	Divider output, pos. terminal. 50 Ω, DC coupled, external decoupling cap. required
24	DIVen	Divider enable input, low-active CMOS input with internal 100-kΩ pull-down resistor
9 - 16, 25 - 32	NC	Not connected. These pins may be connected to ground. Performance will not be affected.
1,8, 17	GND	Ground pins, also connected to the exposed die attach pad.
(33)	GND	Exposed die attach pad of the QFN package, must be soldered to ground.

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply voltage	V_{CC}		3.6	V	to GND
DC voltage at tuning inputs	V_{Vt}	-0.3	V_{CC} + 0.3	V	Inputs Vt0, Vt1, Vt2, Vt3
DC voltage at enable inputs	V_{EN}	-0.3	V_{CC} + 0.3	V	Inputs DIVen, RXen
Junction temperature	T_J	-50	150	°C	
Storage temperature range	T_{STG}	-65	150	°C	
ESD robustness	V_{ESD}		1.2	kV	Human body model, HBM [1)]

1) CLASS 1C according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning inputs	V_{Vt}	0	V_{CC}	V	Inputs Vt0 – Vt3
DC voltage at enable inputs	V_{EN}	0	V_{CC}	V	Inputs DIVen, RXen

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
Thermal resistance, junction-to-ambient	R_{thja}	-	-	50	K/W	JEDEC standard JESD-51-5

4.4 Electrical Characteristics

T_A = -40 °C to +85 °C unless otherwise noted. Typical values measured at T_A = 25 °C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
DC Parameters						
Supply current consumption	I_{CC}		128	155	mA	RX and divider enabled
DIVen input voltage, low level	V_{DIVen_L}	0		0.3 × V_{CC}	V	Input DIVen
DIVen input voltage, high level	V_{DIVen_H}	0.7 × V_{CC}		V_{CC}	V	Input DIVen
RXen input voltage, low level	V_{RXen_L}	0		0.5 × V_{CC}	V	Input RXen
RXen input voltage, high level	V_{RXen_H}	V_{CC} -0.4		V_{CC}	V	Input RXen
VCO tuning voltage	V_{VT}	0		V_{CC}	V	Inputs Vt0 – Vt3
RF Parameters						
VCO start frequency	f_{TX}	117.8	119.3	120.8	GHz	Vt0 = Vt1 = Vt2 = Vt3 = 0
VCO stop frequency	f_{TX}	124.3	125.8	127.3	GHz	Vt0 = Vt1 = Vt2 = Vt3 = 3.3 V
VCO tuning full bandwidth	Δf_{TX}	5.5	6.5	7.5	GHz	Vt0 – Vt3 interconnected
Number adjustable of frequency bands			8			Vt1 – Vt3 used for band switching
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		27		MHz/V	
Phase noise	P_N		-90	-88	dBc/Hz	at 1 MHz offset
Transmitter output power	P_{TX}	-7	-3	1	dBm	Measured without antennas
Divider ratio of TX signal	N_{DIV}		64			
Divider output power	P_{DIV}	-10		-7	dBm	Note 1
Divider output frequency	f_{DIV}	1.85		1.98	GHz	
Receiver gain			8	10	dB	Measured without antennas
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		500		Ω	Differential outputs
IQ amplitude imbalance			tbd		dB	
IQ phase imbalance		-10		10	deg	
Noise figure (DSB)			8.7		dB	Simulated, at f_{IF} = 1 MHz)
Input compression point	1dB ICP		-20		dBm	Measured without antennas

Note 1 Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.

5 Packaging

5.1 Outline Dimensions

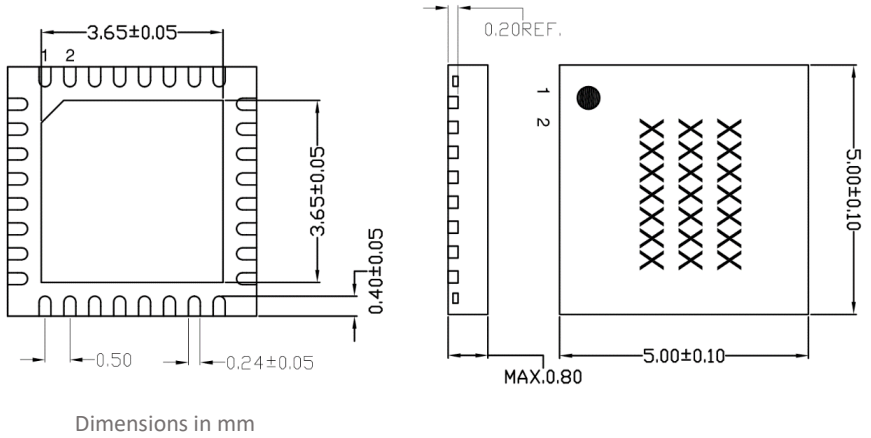


Figure 3 Outline Dimensions of QFN32 Package with Exposed Pad

5.2 Package Code

Top-Side Markings	TRA002
	YYWW

5.3 Antenna Position

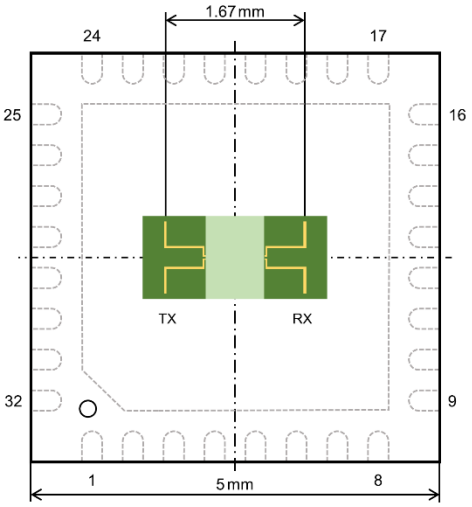


Figure 4 Antenna Position (top view)

5.4 Qualification Test

Table 6 Reliability and Environmental Test

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	pass

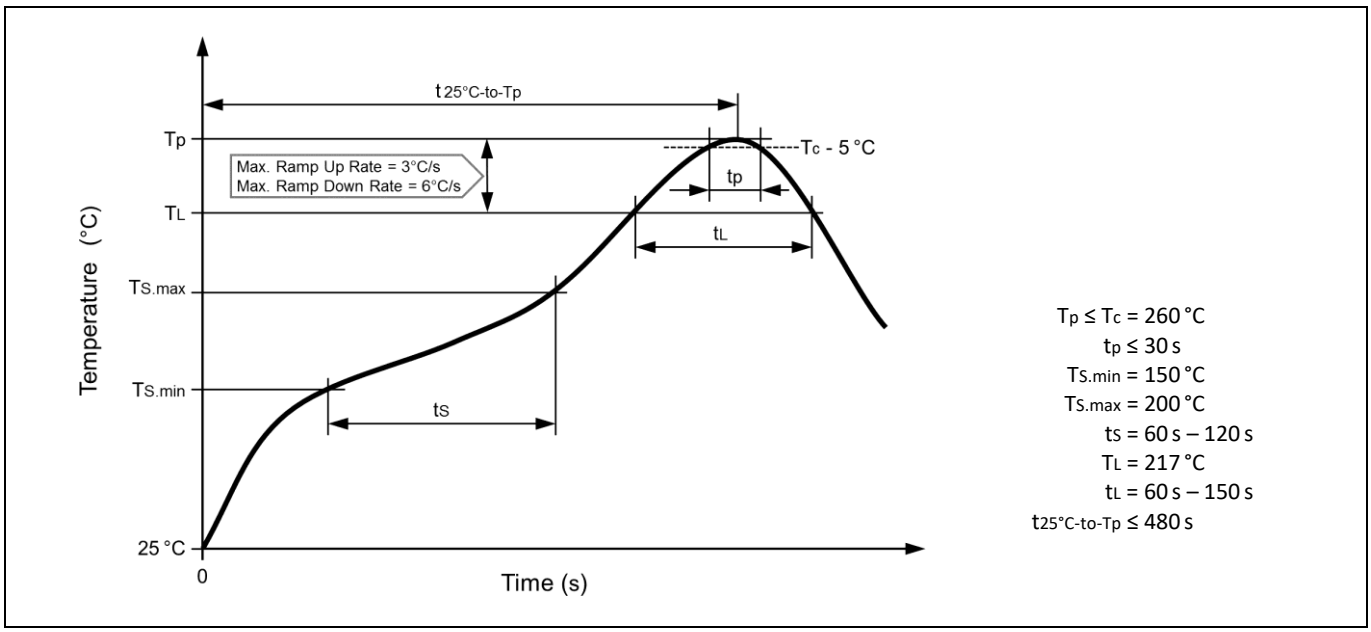


Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

6 Application

6.1 Application Circuit

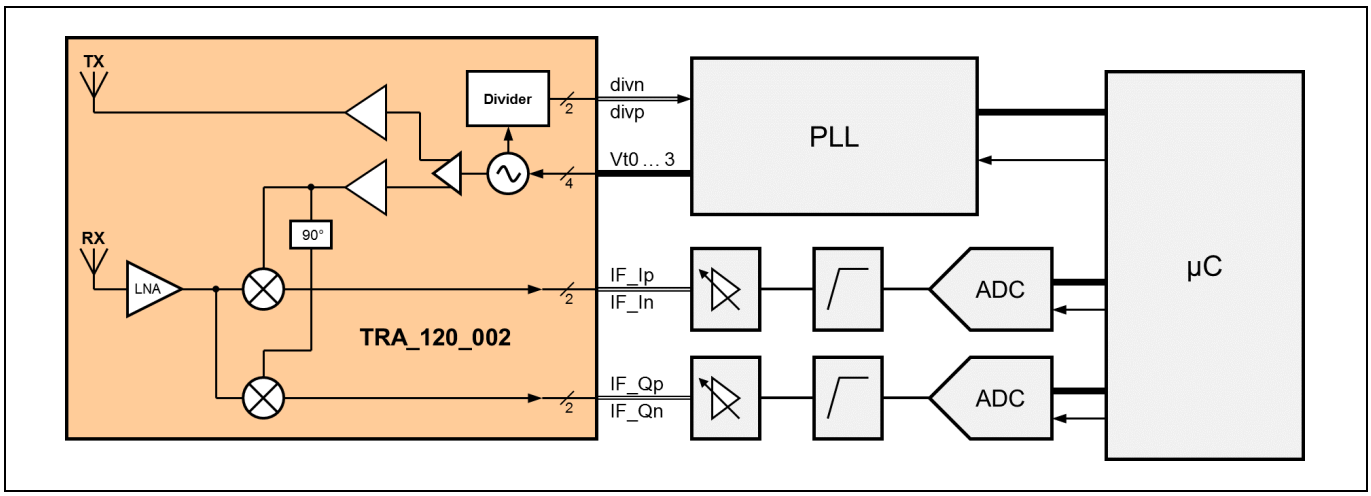


Figure 6 Application Circuit

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Boards

For a quick and easy start into radar development Silicon Radar offers SiRad Easy®. It is an evaluation board system for many of our integrated IQ transceivers with antennas in package or on PCB. It comes with a reference hardware and provides a complete design environment which can be configured via a browser-based graphical user interface. Its rich functionality and the open communication protocol make it a versatile tool – also for enhanced development projects.
It features:

- Distance measurement
- Velocity measurement
- Frequency modulated continuous wave mode (FMCW)
- Continuous wave mode (CW)

For more information about the features of SiRad Easy® see:
https://www.siliconradar.com

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

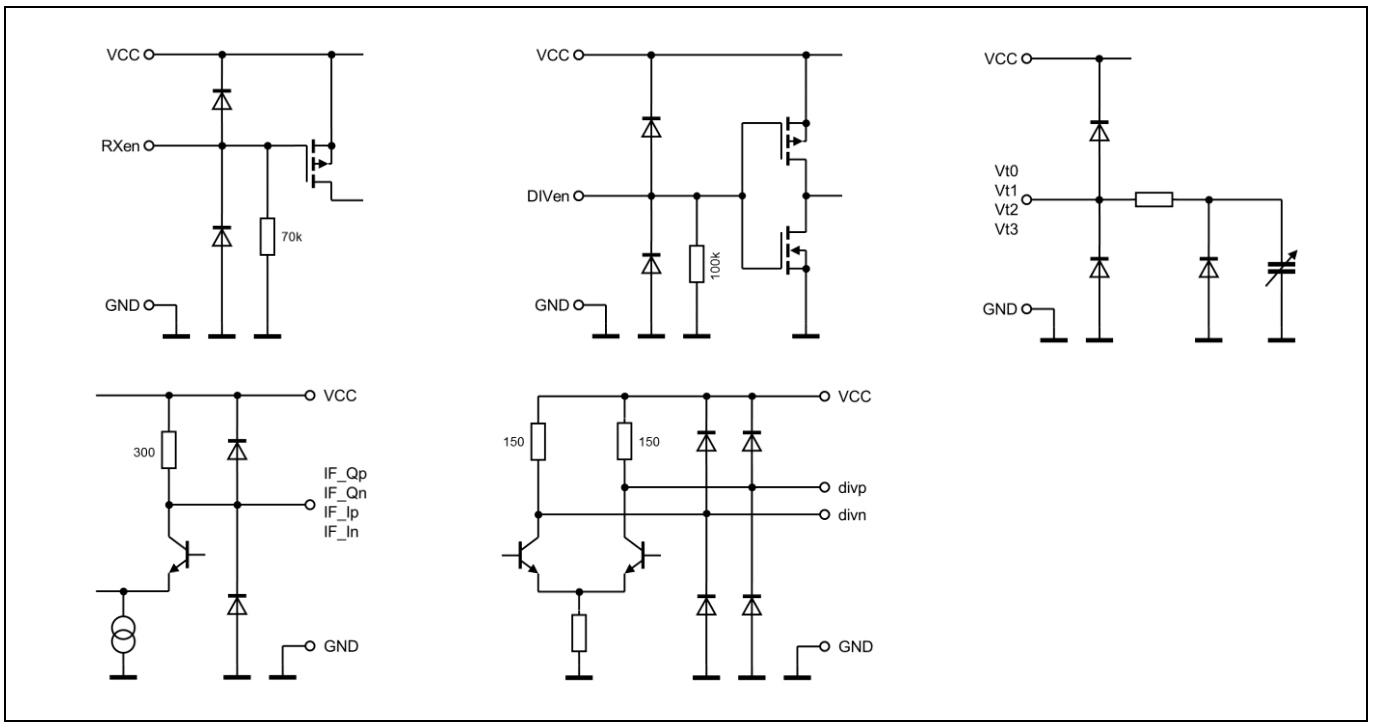


Figure 7 Equivalent I/O Circuits

6.5 VCO Tuning Inputs

The VCO tuning inputs Vt0 – Vt3 are of analog nature, but can be switched digitally as well. The tuning inputs differ in their tuning ranges (tuning bandwidth) and slopes, whereby Vt3 has the widest tuning range, and Vt0 the narrowest.

Table 7 Typical VCO Tuning Bandwidth and Slope

Input	VCO tuning bandwidth (MHz)		Middle band slope (MHz/V)	
Vt0	Δf_{TX_Vt0}	720	$\Delta f_{TX} / \Delta V_{Vt0}$	290
Vt1	Δf_{TX_Vt1}	750	$\Delta f_{TX} / \Delta V_{Vt1}$	300
Vt2	Δf_{TX_Vt2}	1580	$\Delta f_{TX} / \Delta V_{Vt2}$	630
Vt3	Δf_{TX_Vt3}	3450	$\Delta f_{TX} / \Delta V_{Vt3}$	1380

The VCO tuning range of a specific tuning input can be increased by connecting it to another tuning input. All combinations of the four tuning inputs are allowed. Unused tuning inputs must be set to a fixed potential (between 0 and V_{CC}). The interconnection of all inputs Vt0 – Vt3 leads to the maximum tuning bandwidth. For example, if Vt0 is used as tuning input, the variation of the potential at Vt1, Vt2, Vt3 in all logical combinations of 0 and V_{CC}, results in offsetting the tuning curve (see Figure 10).

6.6 Antenna Performance

The simulated gain of TX and RX on-chip antennas shows 10 dBi at an angle of 30°, see Figure 17 and 18.

7 Measurement Results

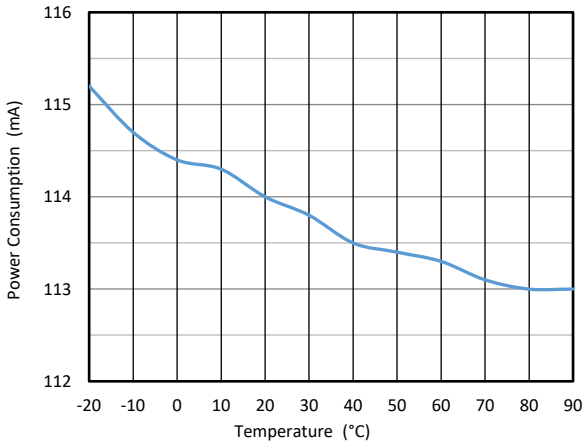


Figure 8 Power Consumption vs. Temperature

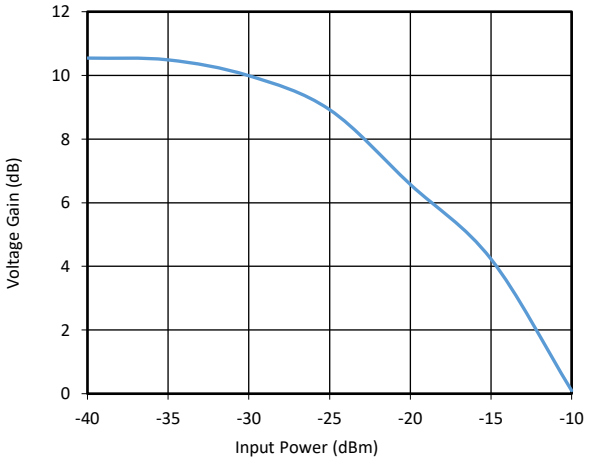


Figure 9 Conversion Gain of the Receiver (without antenna)

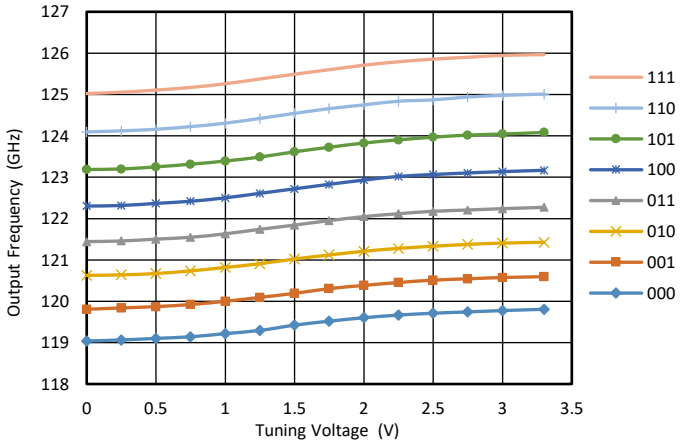


Figure 10 VCO Tuning Curves. Vt0 is varied, while Vt1, Vt2 and Vt3 are driven high or low. For example, 011 means Vt3 = 0, Vt2 = 3.3 V and Vt1 = 3.3 V.

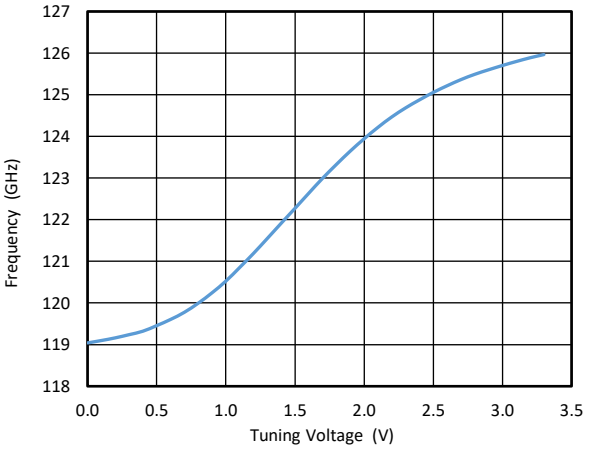


Figure 11 Full Bandwidth VCO Tuning. Vt0, Vt1, Vt2, Vt3 are interconnected. (Vt0 = Vt1 = Vt2 = Vt3)

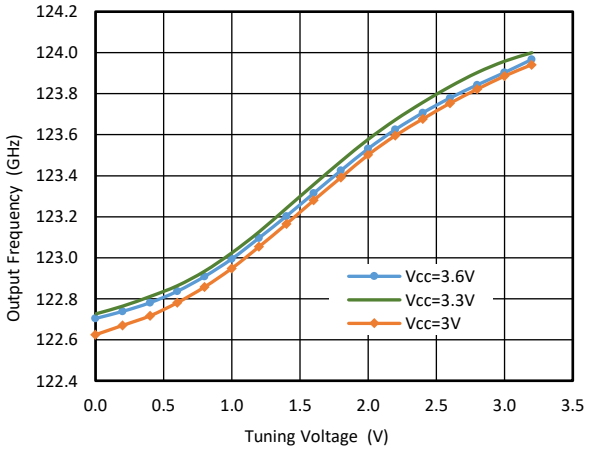


Figure 12 VCO Pushing - V_{CC} ± 300 mV
Vt0 = Sweep , Vt1 = Vt2 = 0, Vt3 = 3.3 V

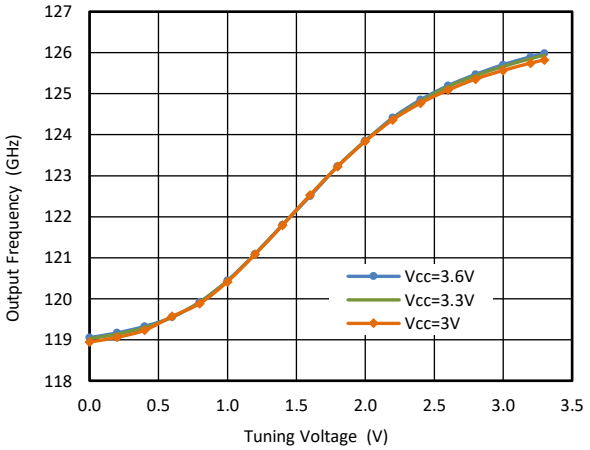


Figure 13 VCO Pushing - Full Bandwidth Operation.
All tuning voltages, Vt0 = Vt1 = Vt2 = Vt3

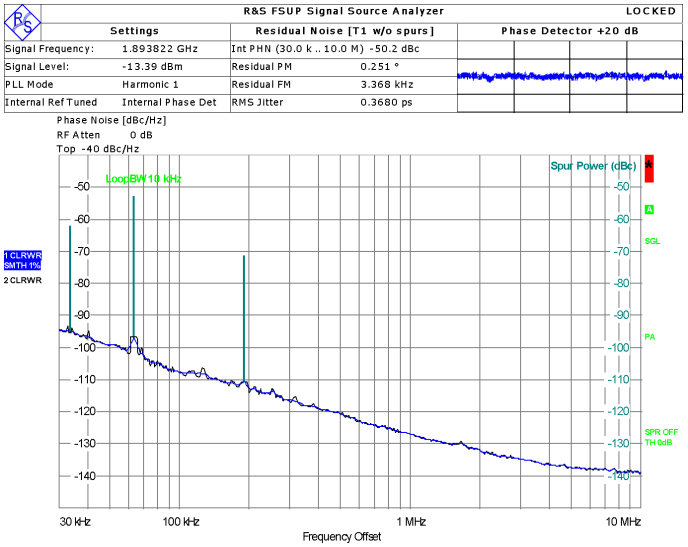


Figure 14 Phase Noise of the Integrated Oscillator at Divider Output (1.89 GHz)

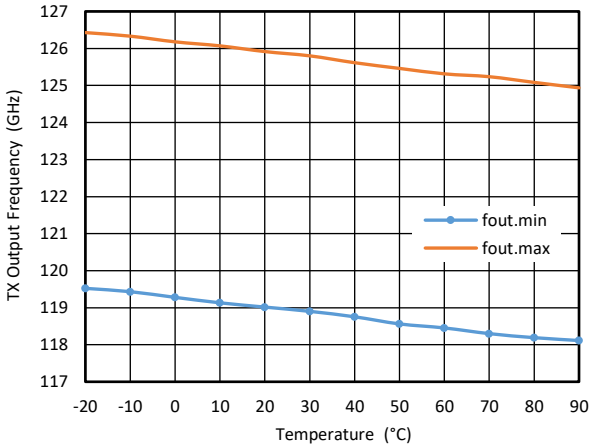


Figure 15 Output Frequency vs. Temperature

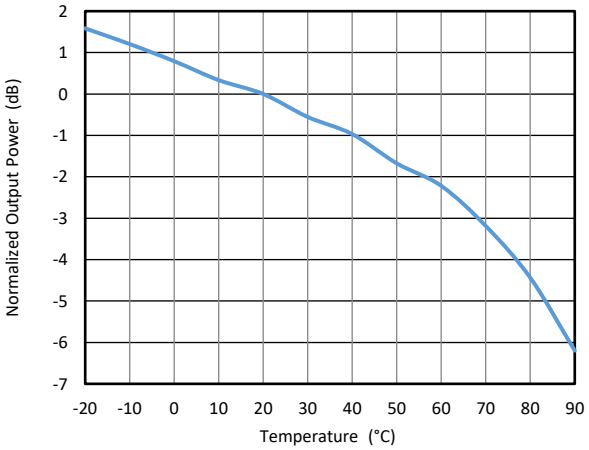


Figure 16 Output Power Swing vs. Temperature (Normalized to 20°C)

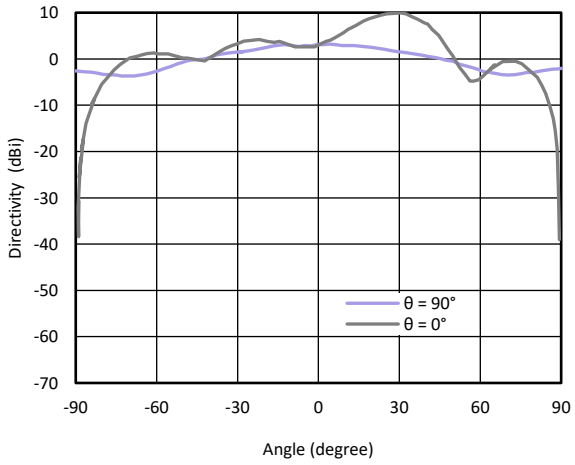


Figure 17 Antenna Radiation Pattern (simulated)

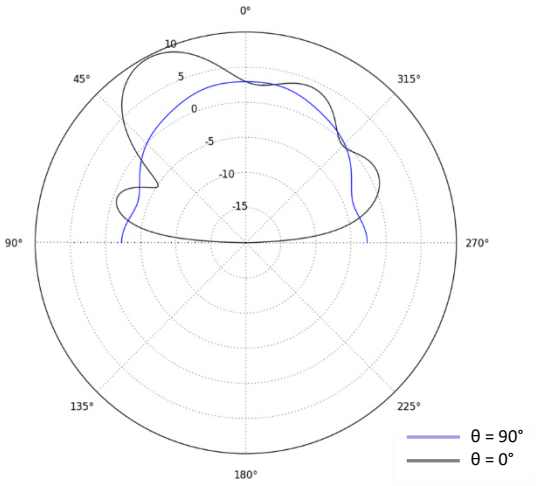


Figure 18 Antenna Radiation Pattern (simulated)

Disclaimer

Silicon Radar GmbH 2018. The information contained herein is subject to change at any time without notice.
Silicon Radar GmbH assumes no responsibility or liability for any loss, damage or defect of a product which is caused in whole or in part by

(i) use of any circuitry other than circuitry embodied in a Silicon Radar GmbH product,
(ii) misuse or abuse including static discharge, neglect, or accident,
(iii) unauthorized modifications or repairs which have been soldered or altered during assembly and are not capable of being tested by Silicon Radar GmbH under its normal test conditions, or
(iv) improper installation, storage, handling, warehousing, or transportation, or
(v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: Silicon Radar GmbH makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any Silicon Radar product and any product documentation. Products sold by Silicon Radar are not suitable or intended to be used in a life support applications or components, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY: BUYER AGREES NOT TO USE SILICON RADAR GMBH'S PRODUCTS FOR ANY APPLICATIONS OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

Silicon Radar GmbH owns all rights, titles and interests to the intellectual property related to Silicon Radar GmbH's products, including any software, firmware, copyright, patent, or trademark. The sale of Silicon Radar GmbH's products does not convey or imply any license under patent or other rights. Silicon Radar GmbH retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by Silicon Radar GmbH. Unless otherwise agreed to in writing by Silicon Radar GmbH, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.