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TRA_120_045

120-GHz Wide-Band IQ Transceiver with Antennas on Chip

Data Sheet

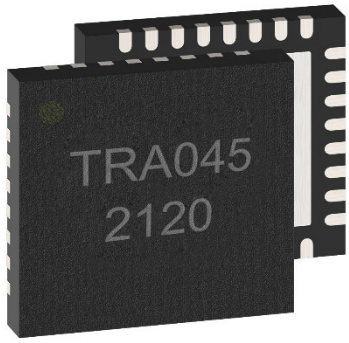
Status:	Date:	Author:	Filename:	
Preliminary	27-Jun-2023	Silicon Radar GmbH	Data_Sheet_TRA_120_045_V0.5	
Version: 0.5	Product number: TRA_120_045	Package: QFN32, 5 × 5 mm²	Marking: TRA045 YYWW	Page: 1 of 16
Document: Annex to VA_U03_01		Anlage 8_Template_Datenblatt_RevE	Date: 19-May-2020	Rev E

Version Control

Version	Changed section	Description of change	Reason for change
0.1	Template, contents	Initial release	
0.2	All sections	Review and update with latest test results	Update following first pre-series fabrication
0.3	Section 4	TX output power revised	Power level specified at output of power amplifier.
0.4	All sections	Principle drawings revised Data according to new measurements updated	Planned revision
0.5	Section 4 and 7	Supply Current and ESD value updated. Antenna measurements included.	Latest measurements typical and maximum values revised, respectively, Antenna characteristics performed in new millimeter-wave chamber.

Table of Contents

1 Features



- Wide-band radar frontend (RFE) with antennas on chip
- Frequency bandwidth of 20 GHz
- Frequency range from 116 GHz to 130 GHz
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Power consumption of 560 mW (full duty cycle)
- Integrated low phase noise VCO
- Receiver with homodyne quadrature mixer
- RX and TX dipole antennas
- QFN32 leadless plastic package 5 × 5 mm²
- Pb-free, RoHS compliant package
- IC is available as bare die as well

1.1 Overview

The radar frontend TRA_120_045 is an integrated wideband transceiver circuit with antennas on chip. It provides a frequency bandwidth of greater than 20 GHz. The circuit includes a low-noise amplifier (LNA), quadrature mixers, a poly-phase filter, a voltage-controlled oscillator, divide-by-64 with differential output and transmit and receive antennas (see Figure 1). The RF signal from the oscillator is directed to the RX path via buffer circuits and polyphase filter to provide quadrature LO signal to the two RX mixers. The RX signal coming from RX antenna is amplified by LNA and converted to baseband by two mixers with quadrature LO signal. The integrated VCO has two analog tuning inputs. These two tuning inputs can be used to obtain the full tuning range of greater than 20 GHz.
The on-chip VCO together with integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With a fixed oscillator frequency, it can be used in continuous wave (CW) mode. Other modulation schemes such as FSK can be implemented by utilizing the analog tuning inputs. The IC is fabricated in a BiCMOS technology.

1.2 Applications

The main application field of the wideband transceiver radar frontend (RFE) without beam focusing element is in short range (in the order of about 5 meters) and high-resolution radar systems. By using dielectric lenses, the range can be increased from a multiple of 10 meters to up to 100 meters. Depending on the measurement target specification a trade-off between measurement resolution and range is required.
The RFE can be used in FMCW mode as well as in CW mode. The transceiver is designed for maximum bandwidth by using two tuning inputs with different tuning ranges and tuning slopes. This makes it possible to extend the bandwidth to the entire tuning range mentioned above.

2 Block Diagram

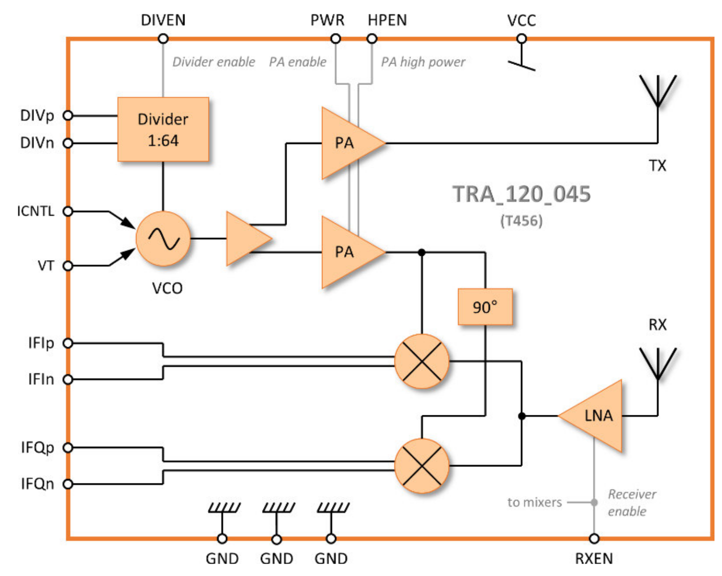


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

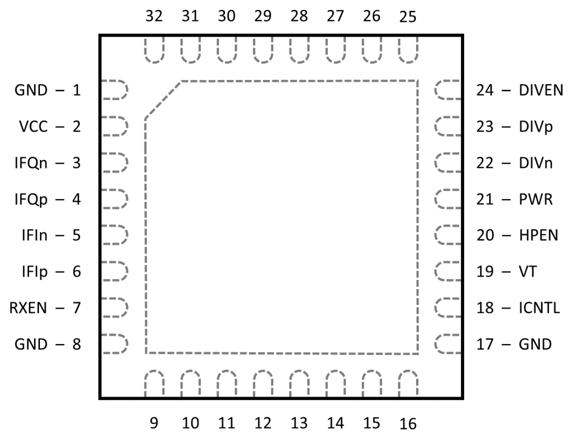


Figure 2 Pin Assignment (QFN32, 5 mm x 5 mm, top view)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
1, 8, 17	GND	Ground
2	VCC	Supply voltage (3.3 V)
3	IFQn	Quadrature IF outputs, DC coupled
4	IFQp	
5	IFIn	
6	IFIp	
7	RXEN	Receiver enable input: 3.3 V – receiver enabled, 0 – receiver off; CMOS input with 100-kΩ pull-up resistor
18	ICNTL	VCO frequency tuning input voltage 0 … 3.3 V, negative characteristic $f_{TX} = f(V_{ICNTL})$
19	VT	VCO frequency tuning input voltage 0 … 4.5 V, positive characteristic $f_{TX} = f(V_{VT})$
20	HPEN	TX high power control: 3.3 V – high power, 0 or open – low power; CMOS input with 100-kΩ pull-down resistor
21	PWR	TX-PA and LO-PA power enable: 3.3 V – on, 0 (or open) – off; CMOS input with 100-kΩ pull-down resistor
22	DIVp	Divider outputs, positive and negative terminal, matched to 50 Ω load, DC coupled, external decoupling capacitor required
23	DIVn	
24	DIVEN	Divider enable input, high-active: 3.3 V – divider enable, 0 – divider off; CMOS input with 100-kΩ pull-down resistor
9 - 16, 25 - 32	NC	Not connected. These pins may be connected to ground. Performance will not be affected
(33)	GND	Exposed die attach pad of the QFN package, must be soldered to ground

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply voltage	V_{CC}		3.6	V	to GND
DC voltage at tuning input VT	V_{VT}	-0.3	4.7	V	
DC voltage at tuning input ICNTL	V_{ICNTL}	-0.3	3.6	V	
DC voltage at enable inputs	V_{EN}	-0.3	V_{CC} + 0.17	V	Inputs RXEN, DIVEN, PWR, HPEN
Junction temperature	T_J		150	°C	
Storage temperature range	T_{STG}	-65	150	°C	
ESD robustness	V_{ESD}		1.0	kV	Human body model, HBM [1)]

1) CLASS 1C according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning input ICNTL	V_{ICNTL}	0	V_{CC}	V	
DC voltage at tuning input VT	V_{VT}	0	4.5	V	
DC voltage at enable inputs	V_{EN}	0	V_{CC}	V	
DC voltage at other inputs	V_x	0	V_{CC}	V	

Note: Do not drive input signals without power supplied to the device.

Power-up sequence should be the following:
1. Connect to ground (optional)
2. Apply V_{CC}
3. Set all control voltages

Power-down sequence should be the reverse of the above.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R_{thja}			30	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

T_A = -40°C to +85°C unless otherwise noted. Typical values measured at T_A = 25°C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
DC Parameters						
Supply current consumption	I_{CC}		170	196	mA	Maximum current with ICNTL = V_{CC}
Enable input voltage, low level	V_{EN_L}	0		0.85	V	
Enable input voltage, high level	V_{EN_H}	2.05	2.15	V_{CC}	V	
VCO tuning voltage	V_{VT}	0		4.5	V	
	V_{ICNTL}	0		V_{CC}	V	
RF Parameters						
TX output start frequency	$f_{TX, min}$	111.5	113.9	115.5	GHz	VT = 0, ICNTL = 3.3 V
TX output stop frequency	$f_{TX, max}$	130.5	134.1	137.2	GHz	VT = 4.5 V, ICNTL = 0
TX tuning full bandwidth	Δf_{TX}	19	22	25	GHz	VT and ICNTL
VCO slope f vs. V for VT	$\Delta f_{TX}/\Delta V_{VT}$		6.33		GHz/V	for f_{TX} = 119 GHz
VCO slope f vs. V for ICNTL	$\Delta f_{TX}/\Delta V_{ICNTL}$		3.9		GHz/V	for f_{TX} = 127 GHz
Transmitter output power (dBm EIRP)	P_{TX_PA}	-8.0	-3.0	+3.5	dBm	Note 1
Output power reduction with HPEN = 0	P_{TX_adj}		3		dB	
Divider output power	P_{div}	-8	-5	-2	dBm	Note 2
Divider output frequency	f_{div}	1.73	1.9	2.15	GHz	
Phase Noise at 1.9 GHz, 1 MHz offset	P_N	-127	-125	-116	dBc/Hz	Measured at divider output
RX conversion gain	RXgain		11.5		dB	Simulated value at 122 GHz
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		600		Ω	Differential output
IQ amplitude imbalance		-1.8		+1.8	dB	
IQ phase imbalance		-10		10	deg	
Receiver Noise figure (DSB)			9		dB	Simulated at 122 GHz.
Input compression point	1dB		-14		dBm	Simulated

Note 1: Typical value of 'Transmitter output power' is average value for f_{TX} = 116 – 134 GHz

Note 2: Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50-Ω match is required in application.

5 Packaging

5.1 Outline Dimensions

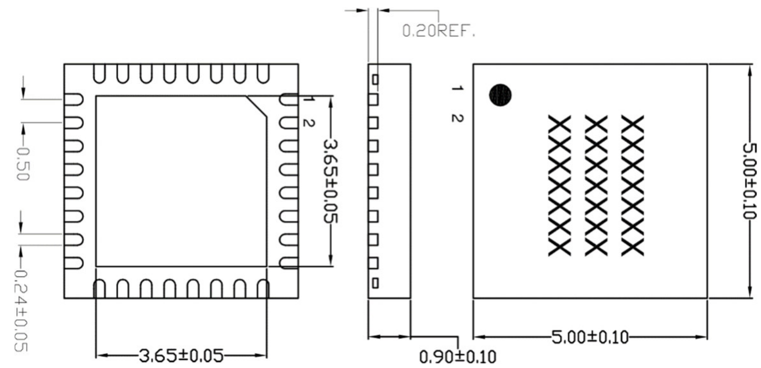


Figure 3 Outline Dimensions of QFN32 Package with Exposed Pad

5.2 Package Code

Top-Side Markings	TRA045 YYWW

5.3 Antenna Position

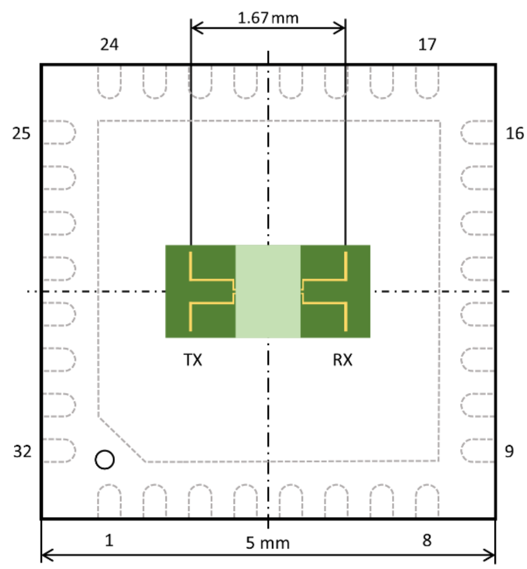


Figure 4 Antenna Position (top view)

6 Application

6.1 Application Circuit Schematic

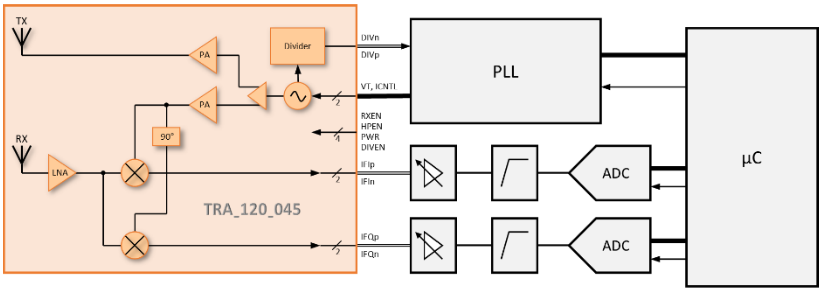


Figure 5 Application Circuit

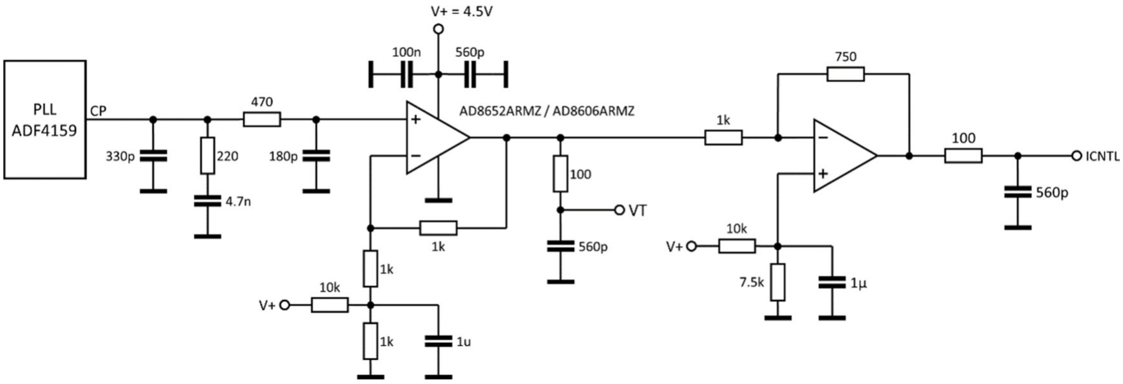


Figure 6 Suggested schematic of a loop filter and generation of control voltages VT, ICNTL for full bandwidth operation

6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling can be implemented with voltage rise times between 10 and 100 µs. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Kit

Silicon Radar offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: https://www.siliconradar.com/evalkits/.

The *SiRad Easy® r4* platform supports development for many of Silicon Radar's integrated IQ transceivers including radar front end boards for TRA_120_045. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V, with exception of inputs VT (max. rating 4.7 V) and ICNTL (max. rating 3.6 V), see section *4.1 Absolute Maximum Ratings*. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

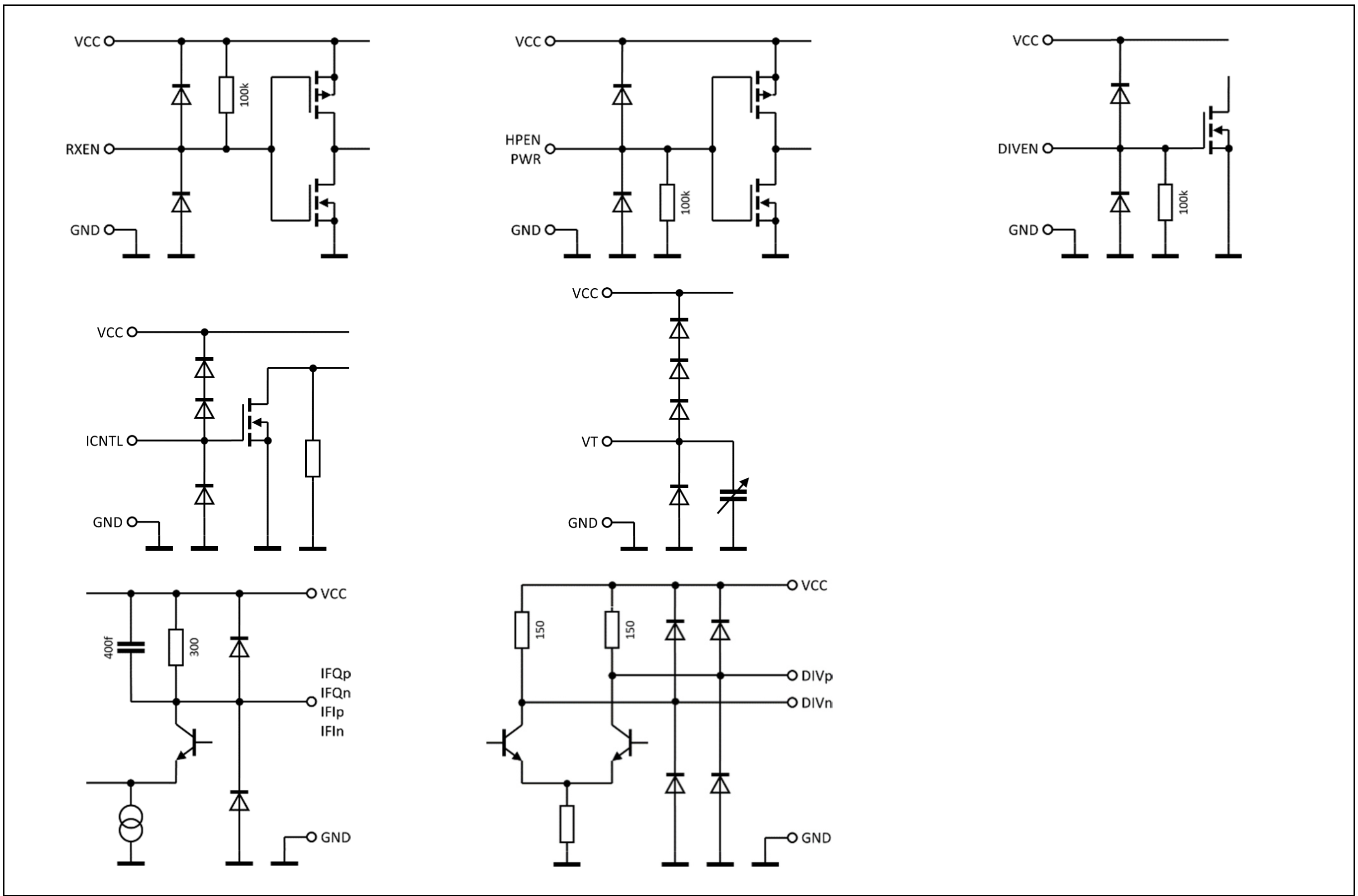


Figure 7 Equivalent I/O Circuits

7 Measurement Results

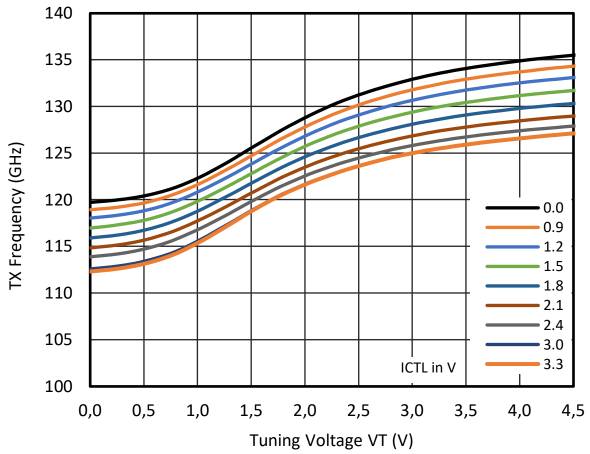


Figure 8 VCO tuning with input VT

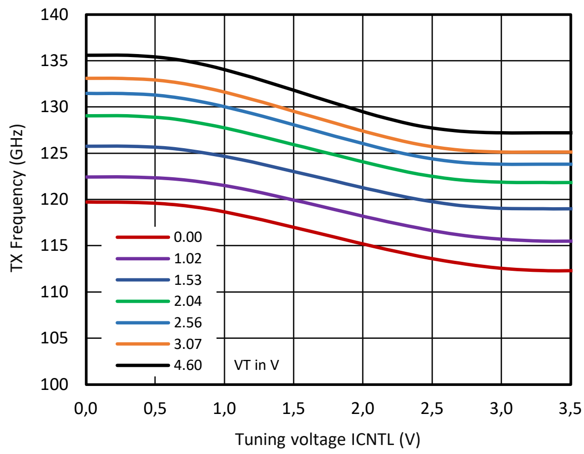


Figure 9 VCO tuning with input ICNTL

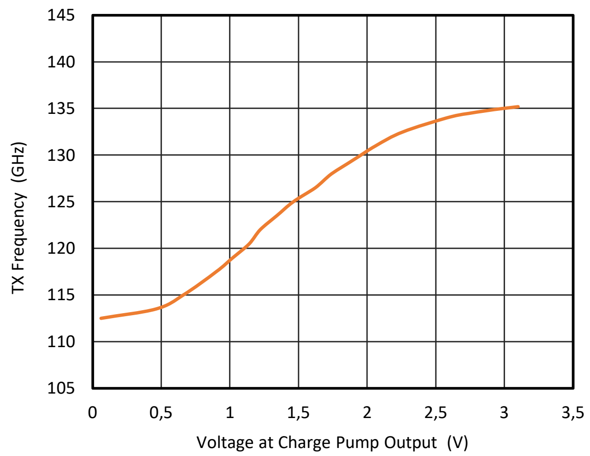


Figure 10 VCO tuning using suggested control circuitry shown in Figure 6, 'Suggested schematic of a loop filter… '

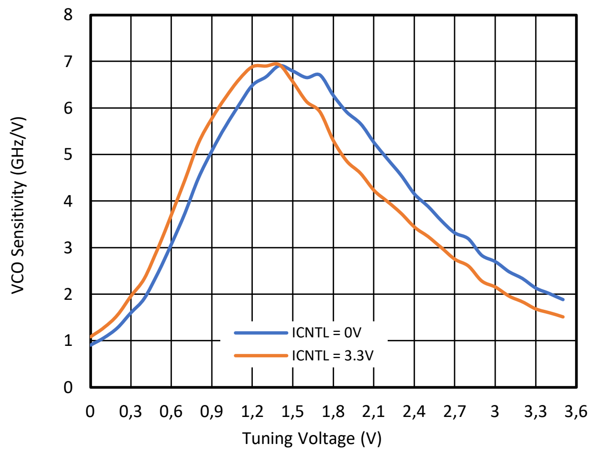


Figure 11 VCO sensitivity with tuning voltage V_{VT}

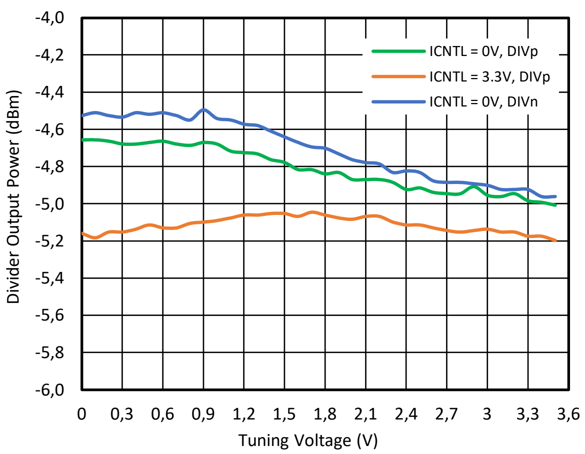


Figure 12 Divider output power with tuning voltage V_{VT} measured single ended divider output DIVp

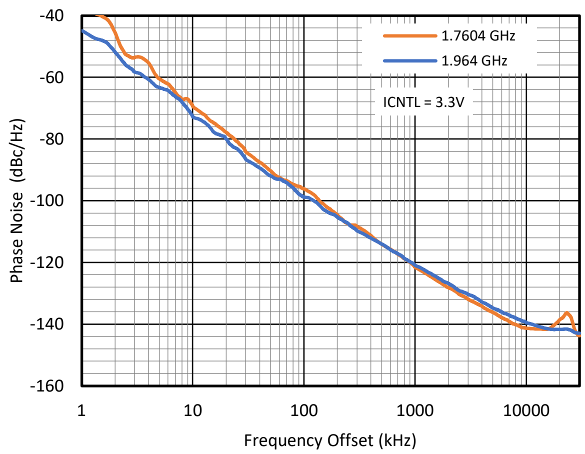


Figure 13 Phase noise at frequency offset at divider output for f_{TX} = 112.6 GHz and f_{TX} = 125.7 GHz

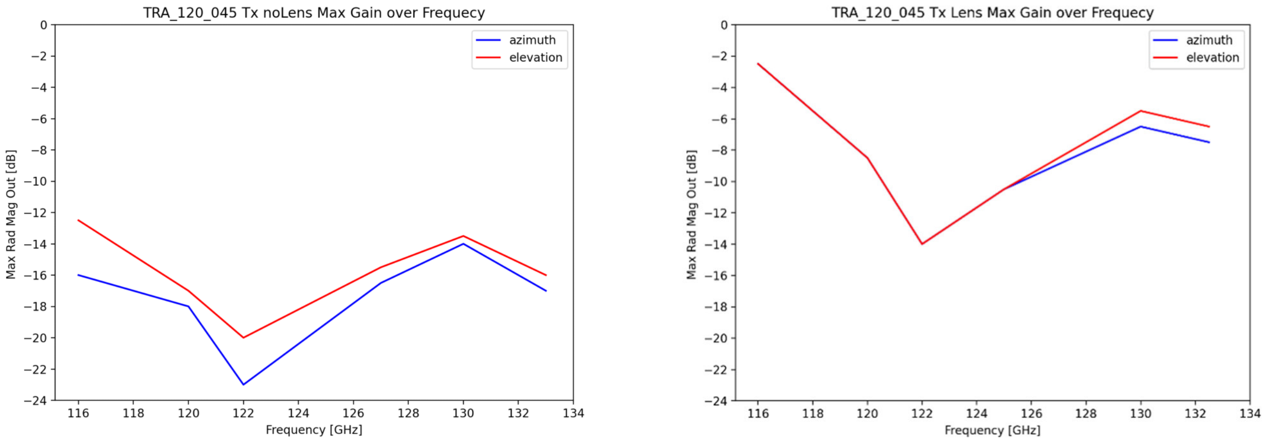


Figure 14 TX gain measured without (left) and with (right) lens vs. frequency

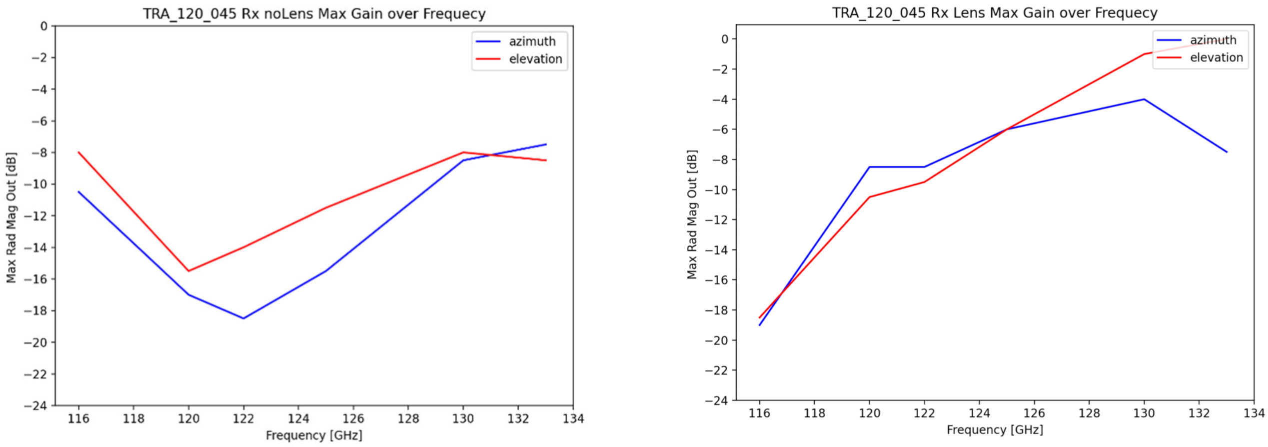


Figure 15 RX gain measured without (left) and with (right) lens vs. frequency.

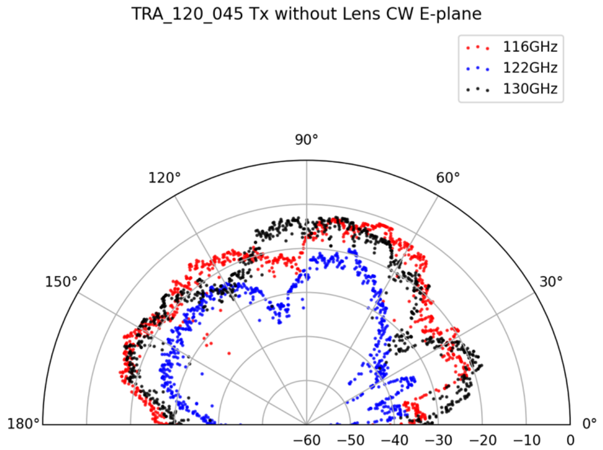


Figure 16 TX Antenna Characteristics in E-plane, measured w/o lens in CW-Mode of operation

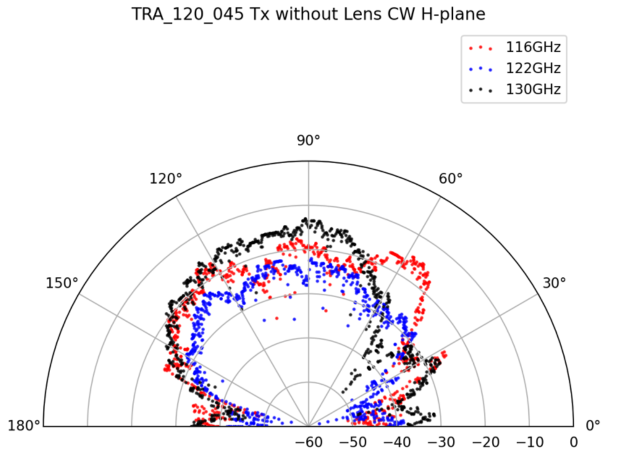


Figure 17 TX Antenna Characteristics in H-plane, measured w/o lens in CW-Mode of operation

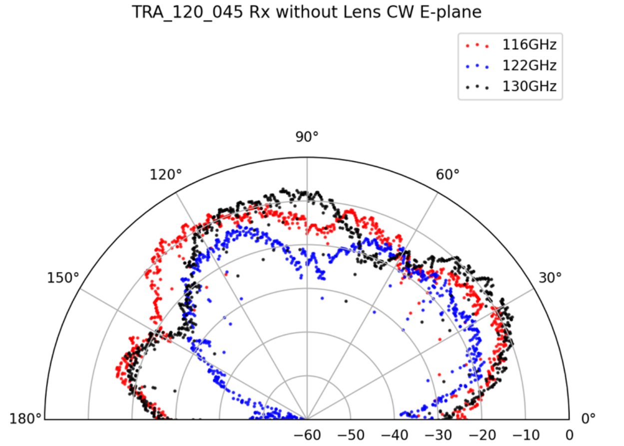


Figure 18 RX Antenna Characteristics in E-plane, measured w/o lens in CW-Mode of operation

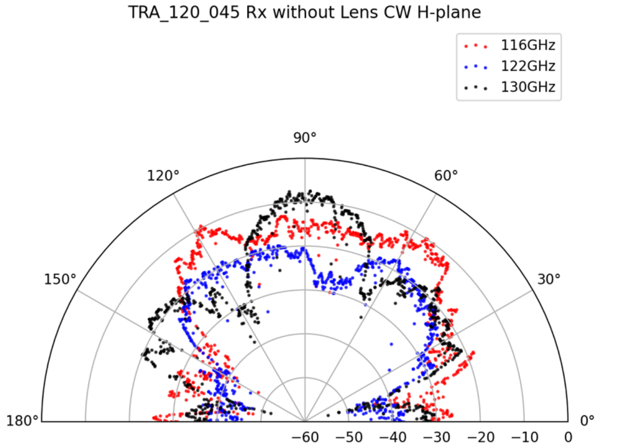


Figure 19 RX Antenna Characteristics in H-plane, measured w/o lens in CW-Mode of operation

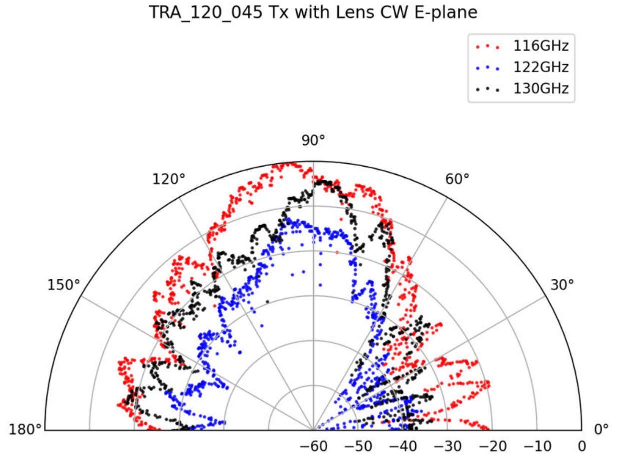


Figure 20 TX Antenna Characteristics in E-plane, measured with lens in CW-Mode of operation

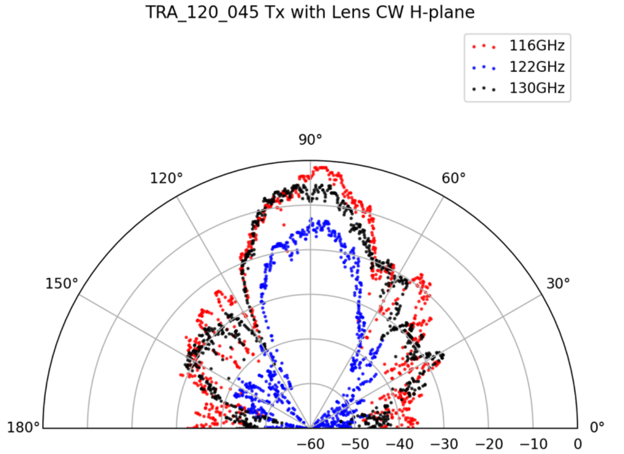


Figure 21 TX Antenna Characteristics in H-plane, measured with lens in CW-Mode of operation

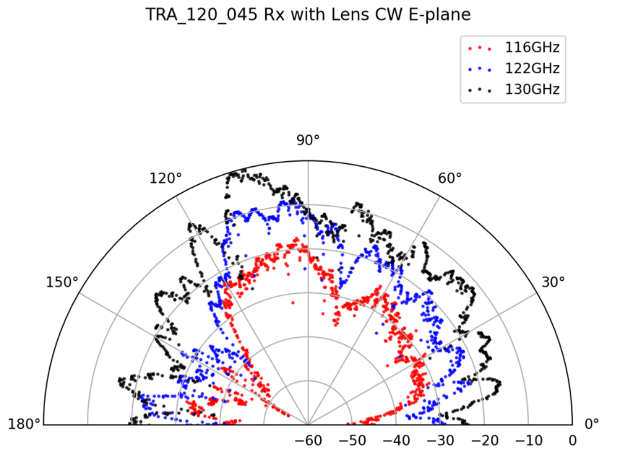


Figure 22 RX Antenna Characteristics in E-plane, measured with lens in CW-Mode of operation

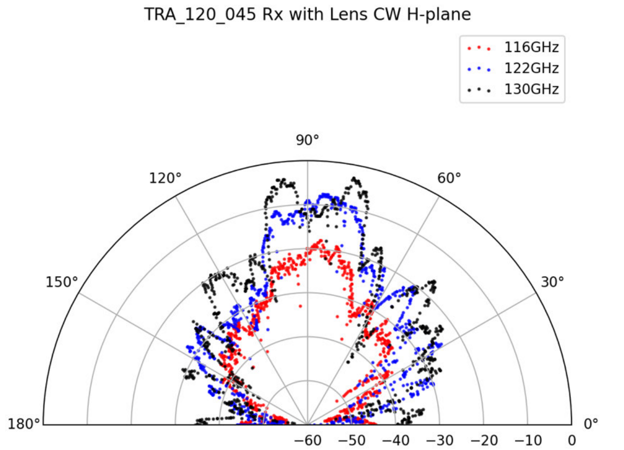


Figure 23 RX Antenna Characteristics in H-plane, measured with lens in CW-Mode of operation

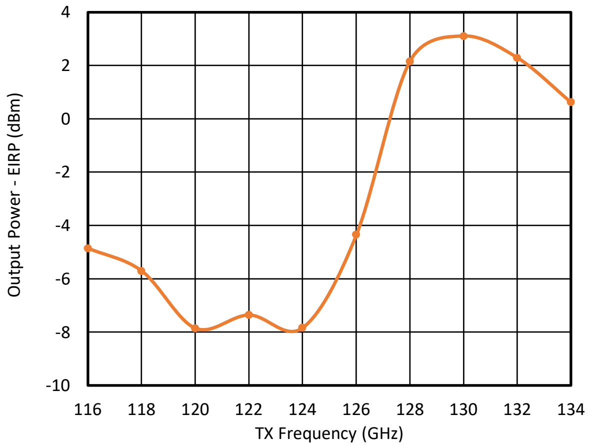


Figure 24 TX output power (EIRP) vs frequency, measured w/o lens in CW-Mode of operation.

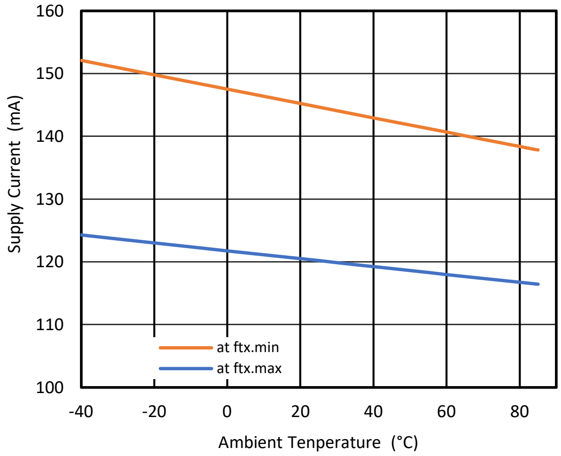


Figure 25 Supply Current vs. Ambient Temperature.

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