indie Semiconductor FFO GmbH
Im Technologiepark 1
15236 Frankfurt (Oder)
Germany

fon +49 335 / 228 80 30
fax +49 335 / 557 10 50
dfo.support@indiesemi.com

TRA_240_097

240 GHz Highly Integrated Radar Transceiver with Antenna on Chip

Preliminary Datasheet

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1 Features

- Radar front end (RFE) with on-chip antenna
- Wide bandwidth of 45 GHz in frequency band of ISM band at 245 GHz
- Integrated low phase noise VCO with injection locking feature
- External LO input
- Receiver with homodyne mixer
- Fully ESD protected device
- Chip can be cascaded in a massive MIMO system
- QFN 40 pin package, 5mm x 5mm with 0.4mm pitch, Pb-free, RoHS compliant
- Device is available as standalone integrated circuit,
- or on Radar Front End for evaluation with Evalkit Easy r4 and optionally with lens

1.1 Overview

The radar front end TRA_240_097 is an integrated transceiver circuit for 240 GHz operation with on-chip antenna. It includes a voltage-controlled oscillator, divide-by-8 frequency divider, an SPDT switch, a frequency multiplier-by-9 chain, frequency doublers, mixers, a low-noise amplifier, a power amplifier, antenna-coupler and integrated antenna (see Figure 1). For proper functionality, a lens must be placed on top of the chip. The lens can be provided. The RF signal from the oscillator is amplified and fed to the frequency multiplier-by-9 chain, a doubler , and via a coupler to the integrated antenna. The RF signal from the oscillator is also directed to the RX path via amplifier and frequency doubler. The RX signal from the antenna is converted to baseband by a mixer with multiplied LO-signal.
The 13.5 GHz VCO has two analog tuning inputs with different tuning ranges and tuning slopes. Both tuning inputs have to be used to obtain the wide RF frequency tuning range of 45 GHz. The analog tuning inputs together with the integrated frequency divider and external fractional-N PLL can be used for frequency modulated continuous wave (FMCW) radar operation. With fixed oscillator frequency it can be used in continuous wave (CW) mode. Other modulation schemes are possible as well by utilizing the analog tuning inputs. The chip can be fed with external LO signal. Many chips can be aligned in a massive MIMO system with external LO or daisy chained using on-chip VCO.
The IC is fabricated in SG13G2 SiGe BiCMOS technology.

1.2 Applications

The main field of application of the 240 GHz transceiver radar front end (RFE) is in short range radar systems which require high range resolution. 45 GHz of bandwidth theoretically gives a radar range resolution down to 6mm in air, and better than 6 mm for other materials with refractive index higher than one. The range resolution is inversely proportional to the refractive index of the material.
The maximum range depends on the gain of the lens that is used, and it can reach several meters. By using lenses with higher gain, the range can be increased.
The RFE can be used in FMCW mode as well as in CW mode.

2 Block Diagram

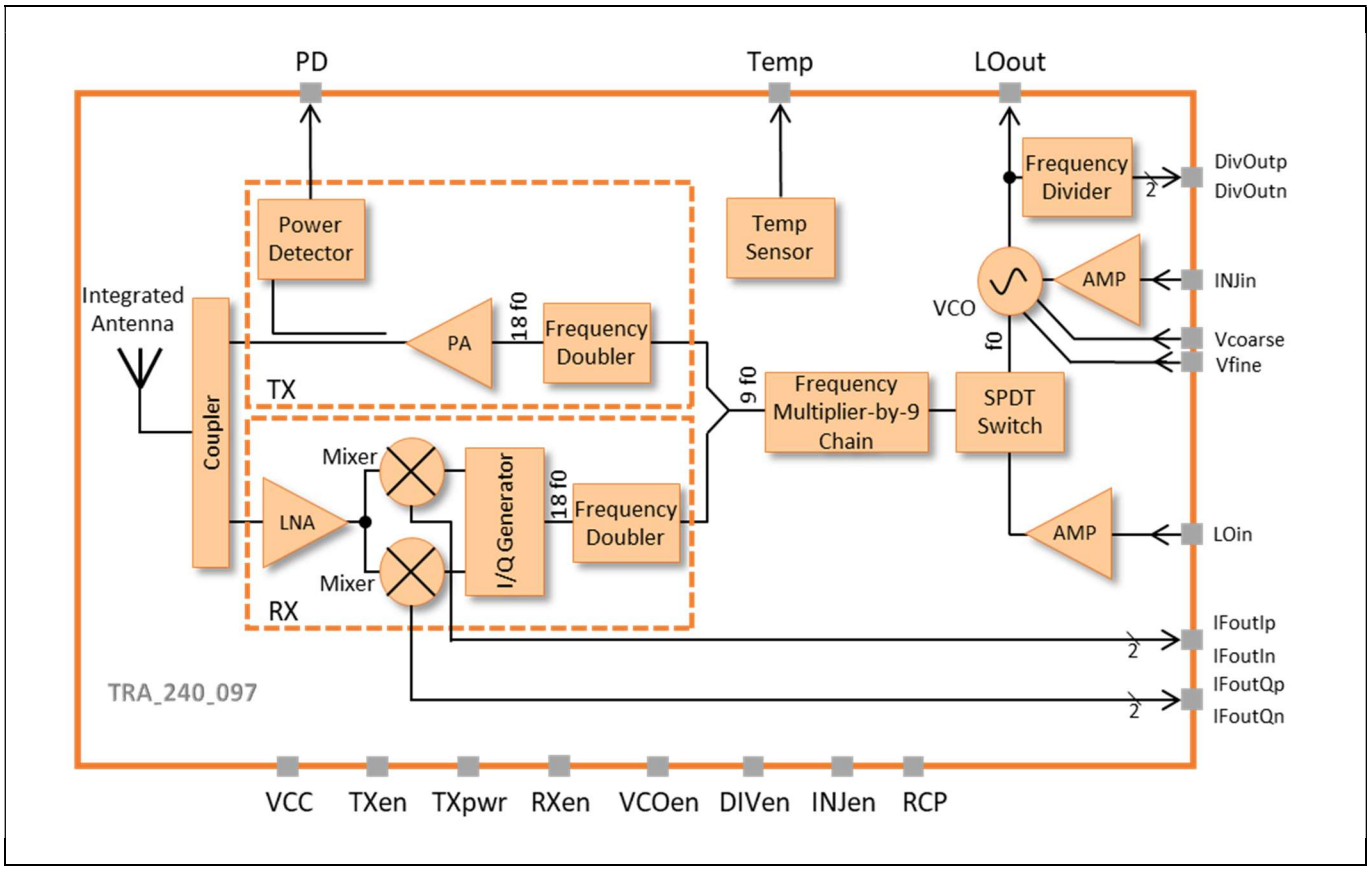


Figure 1 Block Diagram of 240 GHz radar chip TRA_240_097.

3 Pad Configuration

3.1 Pad Assignment

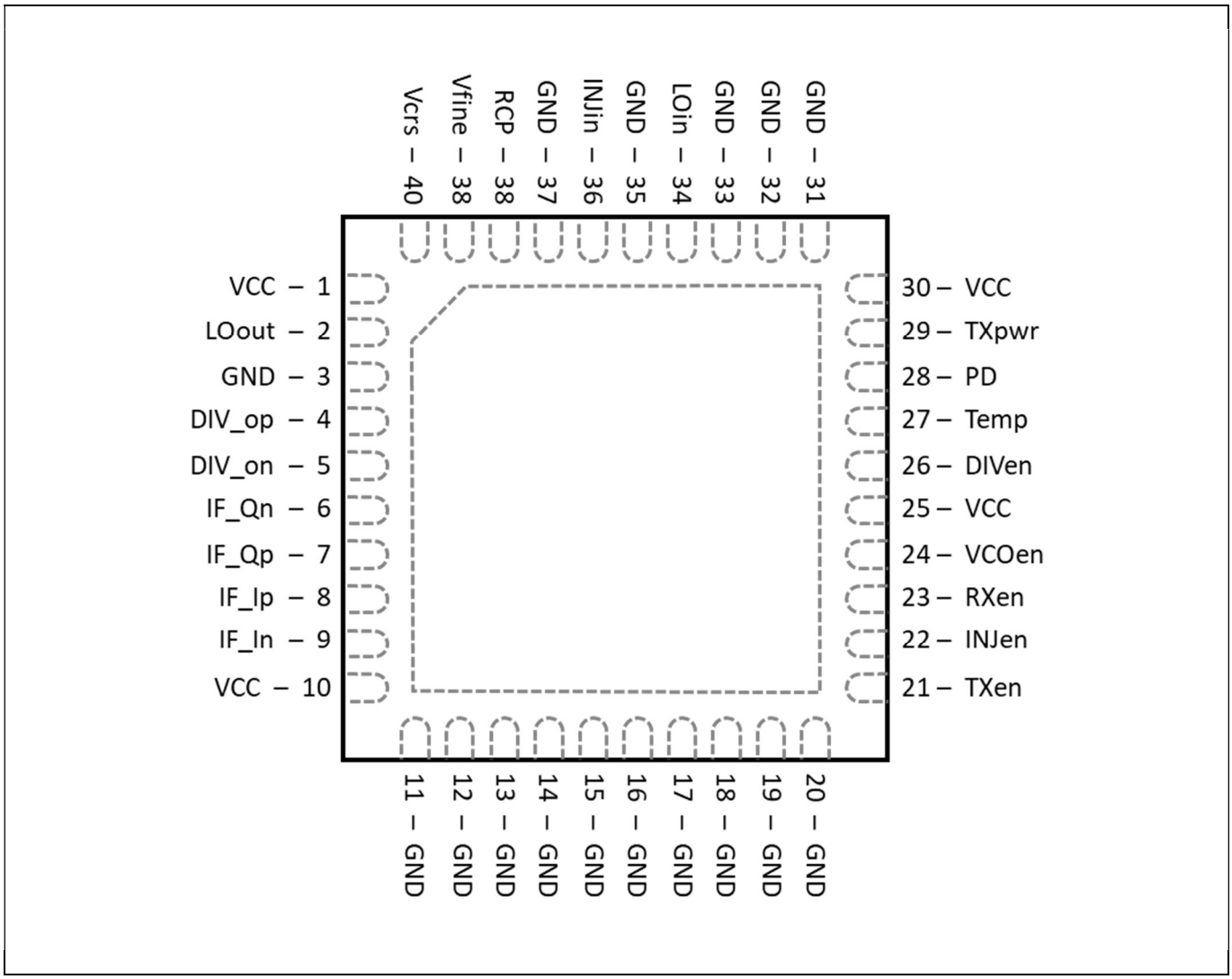


Figure 2 Pad Assignment (Chip Top View)

3.2 Pad Description

Table 1 Pad Description

Pin		Description
No.	**Name**	
1,10,25	VCC	Global Supply: 3.3 V
2	LOout	VCO output RF-signal (single-ended 50 Ω) (12-15 GHz), should be terminated with 50 Ω if not used
4	DivOutp	Divider output (differential 100 Ω) (3-3.75 GHz), DC-coupled, on-board DC-block capacitors are required
5	DivOutn	
6	IF_Qn	IF Q-output, DC-coupled ANALOG Output: DC-coupled low impedance might damage the chip (> 500 Ω)
7	IF_Qp	
8	IF_Ip	IF I-output, DC-coupled ANALOG Output: DC-coupled low impedance might damage the chip (> 500 Ω)
9	IF_In	
21	TXen	TX-blocks (TX120 GHz Amplifier, TX-Doubler, TX-PA) control pin DIGITAL: (3.3V for enable mode, 0V for disabled mode), 50 kΩ pull-down on chip

22	INJen	VCO's injection Amplifier control voltage, DIGITAL: (3.3V for enable mode, 0V for disabled mode), 50 kΩ pull-down on chip
23	RXen	RX-blocks (RX120 GHz Amplifier, RX-Doubler, RX-LNA, RX-IQ Mixers) control pin DIGITAL: (3.3V for enable mode, 0V for disabled mode), 50 kΩ pull-down on chip
24	VCOen	VCO and its Buffer Amplifiers control voltage, DIGITAL: (3.3V for enable mode – VCO is connected to multiplier, 0V for disabled mode – LOinput is connected to multiplier), 50 kΩ pull-down on chip
26	DIVen	Divider control voltage, DIGITAL: (3.3V for enable mode, 0V for disabled mode), 50 kΩ pull-down on chip
27	Temp	Temperature Sensor Output ANALOG Output: DC-coupled low impedance might damage the chip. (> 500 Ω)
28	PD	TX-Power Detector Output ANALOG Output: DC-coupled low impedance might damage the chip. (> 500 Ω)
29	TXpwr	TX-Output Power Control ANALOG Input: Low impedance might damage the chip. 0V: P_{out_max}, 3.3V: P_{out_max}-16dB ; No pull-up/down resistor on chip
34	LOin	External LO input (single-ended 50-ohm) (12-15 GHz), can be left open if not used
36	INJin	12-15 GHz VCO injection input signal (single-ended 50ohm), should be terminated with 50-ohm if not used
38	RCP	VCO Range control DIGITAL: (3.3V for 45 GHz, 0V for 23 GHz), 50kΩ pull-down on chip
39	Vfine	Fine frequency tuning voltage of VCO, 0V to 3.3V, ANALOG.
40	Vcrs	Coarse frequency tuning voltage of VCO, 0V to 3.3V, ANALOG.
3,11-20,26, 31-33,35,37	GND	Global Ground. The IC's internal ground is connected to the exposed die attach pad of the QFN package. This pad must be soldered to PCB ground.

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Supply voltage	V_{CC}		3.6	V	to GND
DC voltage at tuning inputs	V_{Vt}	-0.3	V_{CC} + 0.3	V	Inputs Vfine, Vcrs
DC voltage at enable inputs	V_{EN}	-0.3	V_{CC} + 0.3	V	Inputs TXen, INJen, RXen, VCOen, DIVen, TXpwr, RCP
Junction temperature	T_J	-50	150	°C	
Storage temperature range	T_{STG}		150	°C	
Floor life (out of bag) at factory ambient (30°C / 60% RH)	FL		168	h	IPC/JEDEC J–STD-033A MSL Level 3 Compliant [1)]
ESD robustness	V_{ESD}		500	V	Human body model, HBM [2)]

1) If the devices are stored outside of the packaging, beyond this time limit, the device should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 12 hours.

2) CLASS 1A according to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Remarks / Condition
Ambient temperature	T_A	-40	65	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3 V ± 5%)
DC voltage at tuning inputs	V_{Vt}	0	V_{CC}	V	Inputs Vfine, Vcrs
DC voltage at enable inputs	V_{EN}	0	1.2	V	Inputs TXen, INJen, RXen, VCOen, DIVen, TXpwr, RCP

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit	Remarks / Condition
Thermal resistance, junction-to-ambient	R_{thja}			30	K/W	JEDEC JESD51-5

4.4 Electrical Characteristics

T_A = -40°C to +65°C unless otherwise noted. Typical values measured at T_A = 25°C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
DC Parameters						
Supply current consumption at V_{CC1}	I_{CC1}	tbd	250	tbd	mA	All enabled but INJEN disabled
Enable input voltage, low level	V_{EN_L}	0		0.3	V	
Enable input voltage, high level	V_{EN_H}	2.7	3.3	V_{CC}	V	
VCO tuning voltage	V_{Vt}	0		V_{CC}	V	
RF Parameters						
Start frequency	f_{TX}	tbd	222.5	tbd	GHz	
Stop frequency	f_{TX}	tbd	267.5	tbd	GHz	
Tuning full bandwidth	Δf_{TX}	tbd	45	tbd	GHz	
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		Tbd		MHz/V	
Phase noise	P_N	tbd	-110	tbd	dBc/Hz	at 1 MHz offset, LOout
Transmitter output power	P_{TX}	tbd	0.6	tbd	dBm	Measured on-chip w/o antenna
Divider ratio of TX signal	N_{div}		72			
Divider output power	P_{div}	tbd	-5	tbd	dBm	
Divider output start frequency	f_{div}	tbd	3.09	tbd	GHz	
Divider output stop frequency		tbd	3.715	tbd	GHz	
Receiver gain	g_{RX}	tbd	18	tbd	dB	Measured on-chip w/o antenna
IF frequency range	f_{IF}	0		100	MHz	
IF output impedance	Z_{OUT}		50		Ω	Differential outputs
IQ amplitude imbalance	Aimb	tbd	1	tbd	dB	
IQ phase imbalance	PHimb	tbd	4	tbd	deg	
Noise figure (DSB)	NF	tbd	15.7	tbd	dB	
Input compression point	1dB ICP	tbd	-16.5	tbd	dBm	

Note 1: Measured single-ended. Divider outputs are loaded with 50 Ω, external decoupling capacitors are required. No 50 Ω match is required in application.

4.5 Power-up Sequencing

To prevent damage of IC at switching on or off a specific power-up and power-down sequence has to be followed. Reason is the special ESD-protection circuitry integrated in the chip with high-current diodes between control inputs/outputs and supply voltage pin(s) (see section ESD).

Power-up:

First, all supply voltages must be applied, and then apply control voltages.

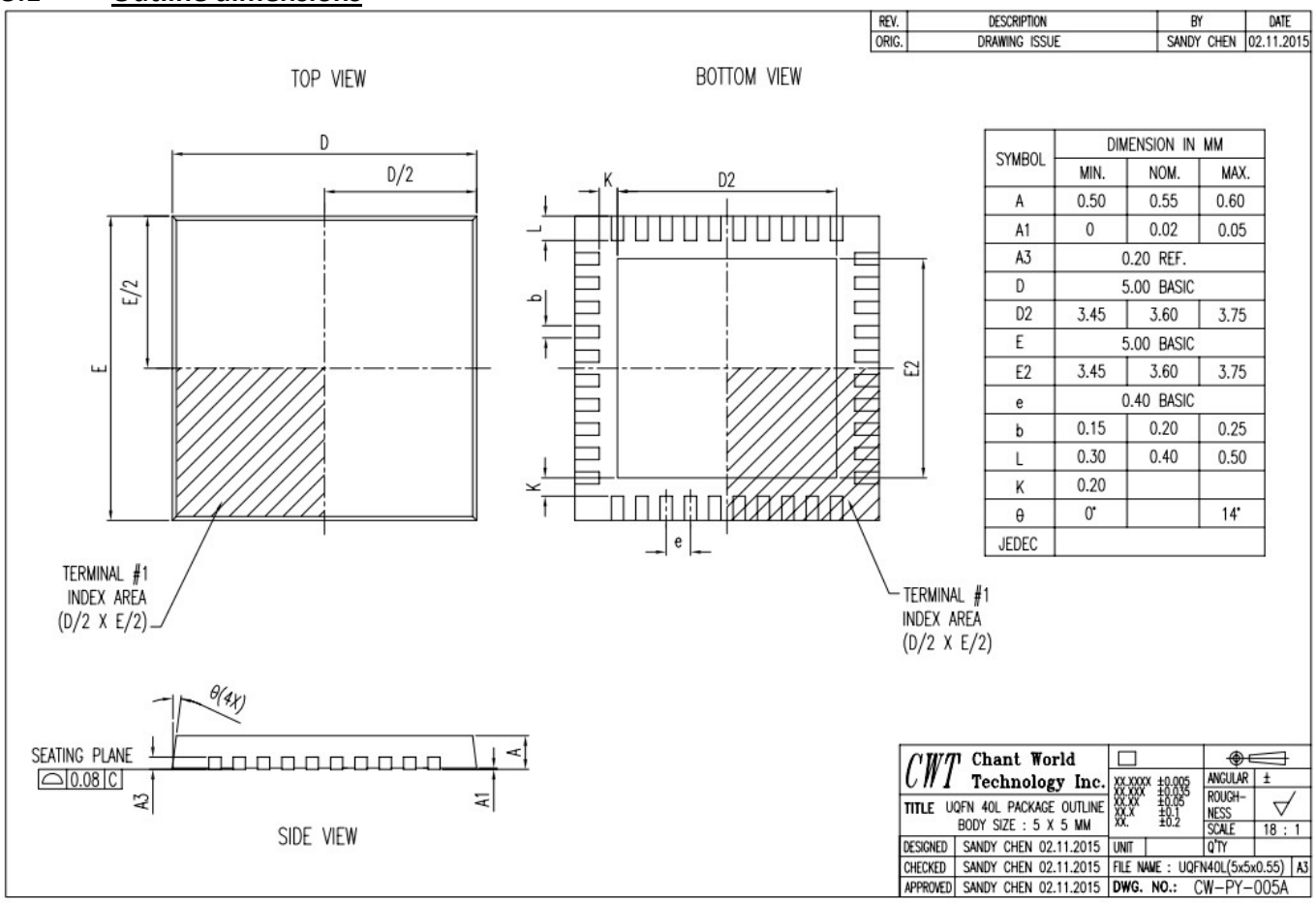
Power-down:

First, switch off all control voltages, then switch off all supply voltages.

To meet the requirements, different sequencing techniques can be applied: sequential power-up, ratiometric power-up or simultaneous power-up. (See for example: http://www.irf.com/technical-info/appnotes/an-1053.pdf)

5 Package

5.1 Outline dimensions



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.20 REF.	
D		5.00 BASIC	
D2	3.45	3.60	3.75
E		5.00 BASIC	
E2	3.45	3.60	3.75
e		0.40 BASIC	
b	0.15	0.20	0.25
L	0.30	0.40	0.50
K	0.20		
θ	0°		14°
JEDEC			

Figure 3 Outline Dimensions of QFN40 Package with Exposed Pad

5.2 Package Code

Top-Side Markings	TRA097 YYWW

5.3 Antenna Position

The position of the radiating center of the integrated antenna is 501 µm off the center of the 5 x 5 mm² package.

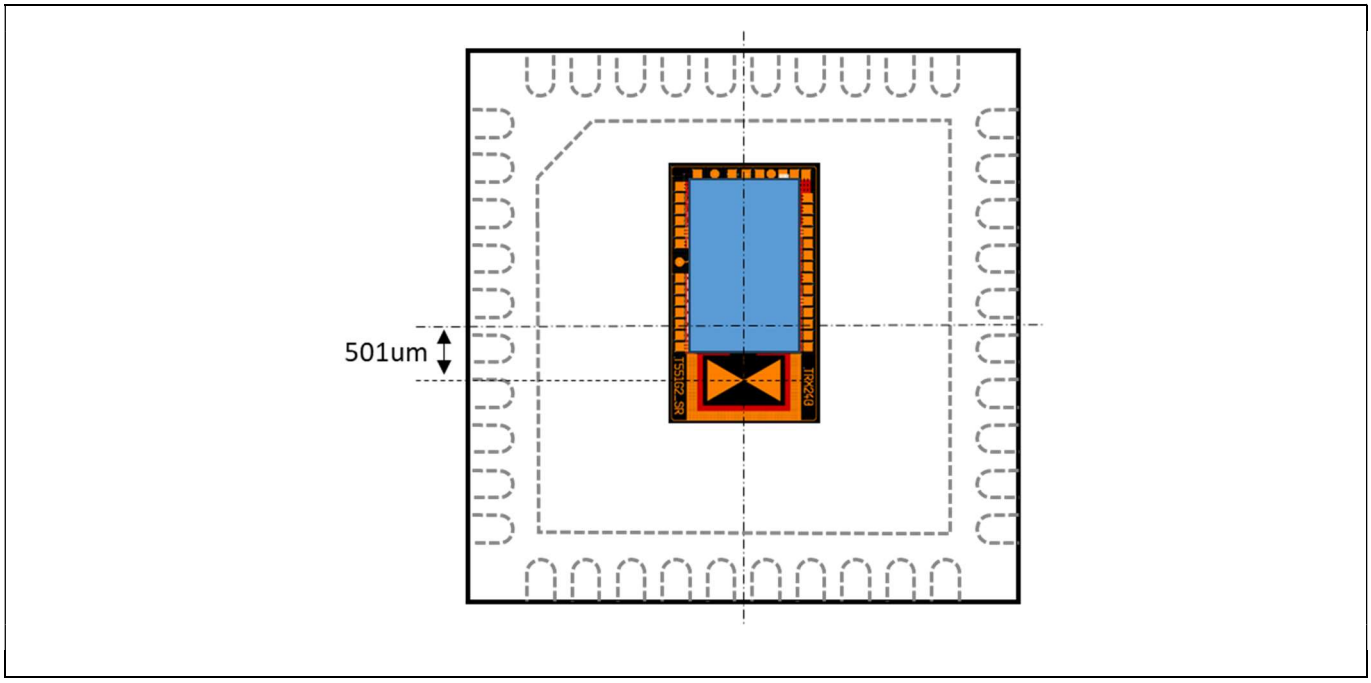


Figure 11 Antenna center vs. package center

6 Application

6.1 Application Circuit Schematic

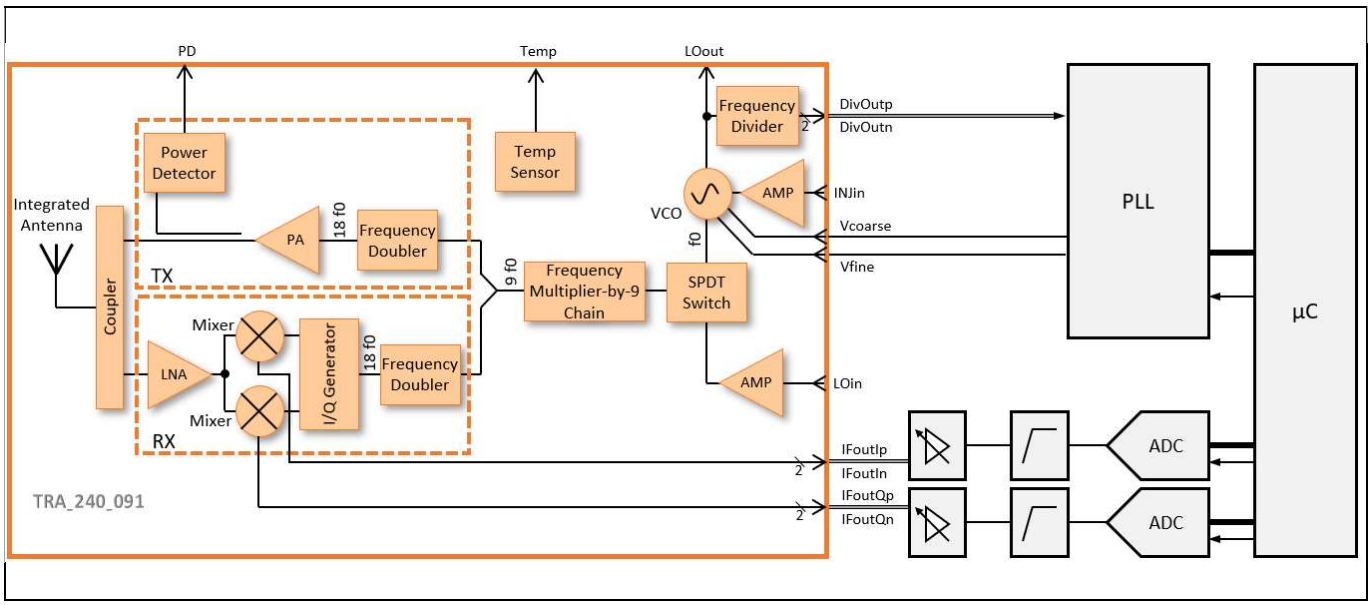


Figure 4 Application Circuit

6.2 Power Cycling

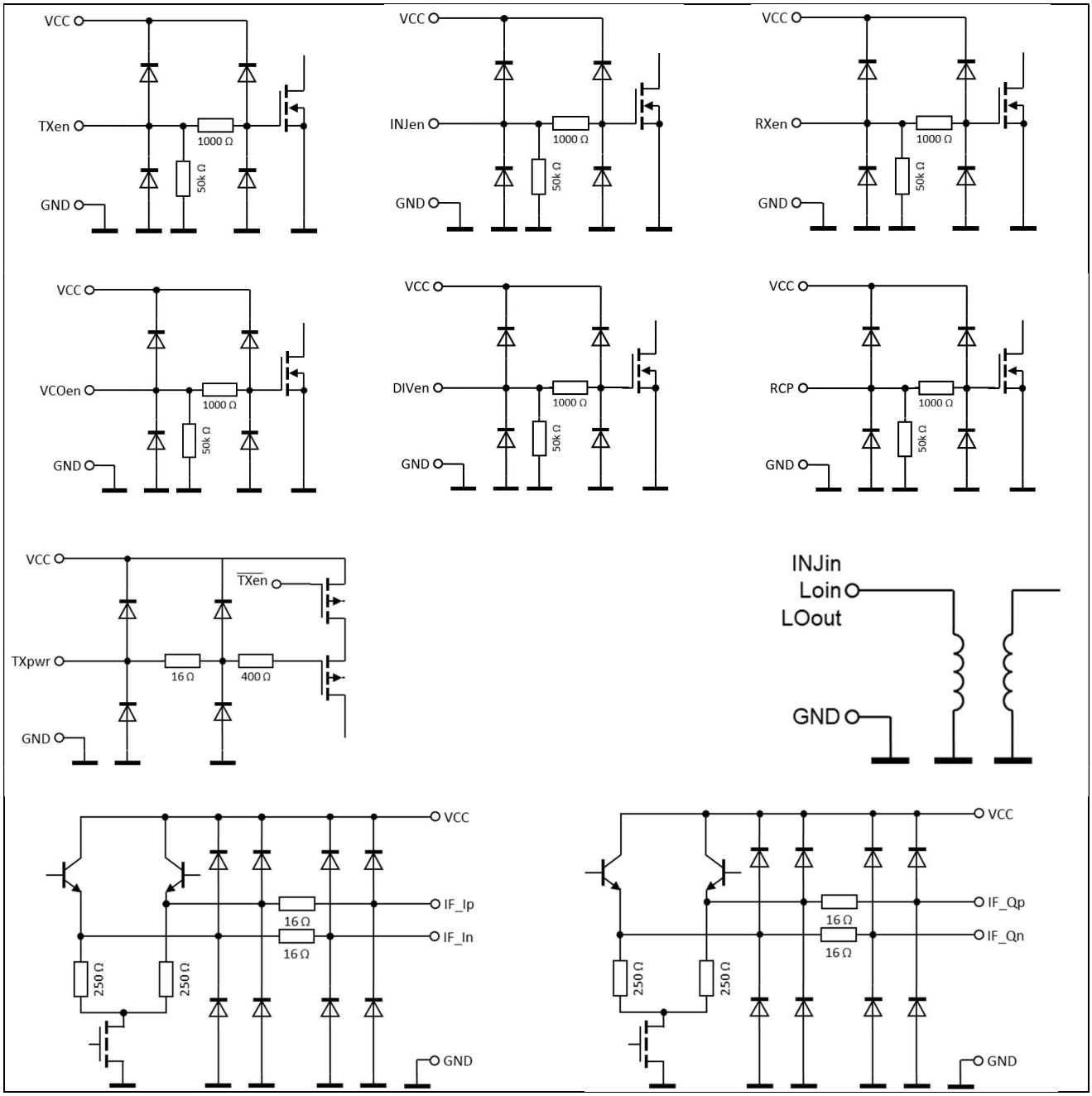
It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

6.3 Evaluation Kit

indie Semiconductor FFO offers evaluation kits for speeding up radar development. Please review our website and product sheets for more information: https://www.indie.inc/radar-portfolio/#eval-kits .
The SiRad Easy® r4 platform supports development for many of indie Semiconductor FFO integrated IQ transceivers including radar front end boards for TRA_240_097. It serves as reference hardware and provides a design environment including a graphical user interface for parameter setting. Its functionality and communication protocol are adaptable to development projects.

6.4 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds V_{CC} by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.



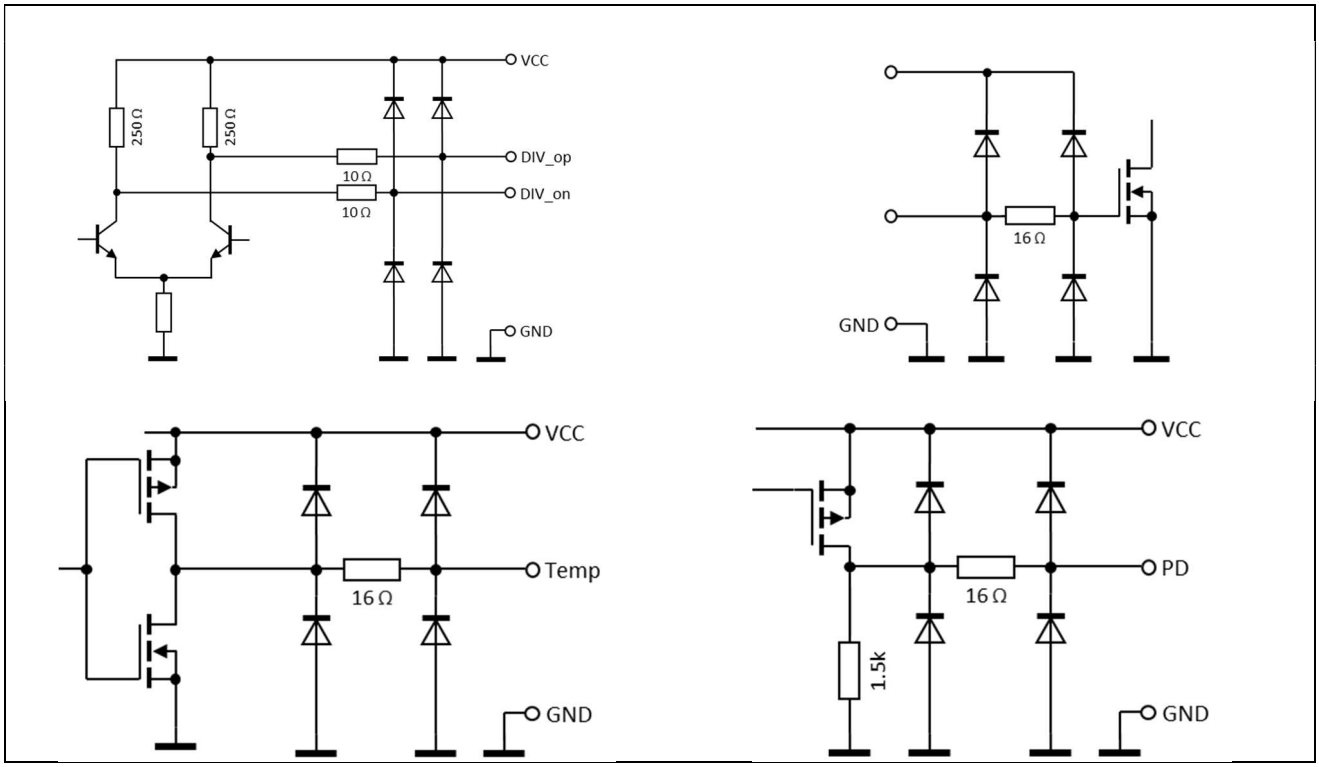


Figure 5 Equivalent I/O Circuits

7 Reliability and Environmental Test

Table 6 Reliability and Environmental Test according to JEDEC Standards (performed for packaged device)

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	tbd
Temperature Cycling	JESD22-A104	850 cycles at -40°C … 125°C	tbd
HTSL	JESD22-A103	1,000 h at 150°C	tbd
HTOL	JESD22-A108	1,000 h at 85°C	tbd
THB	JESD22-A101	1,000 h at 85°C and 85% RH	tbd

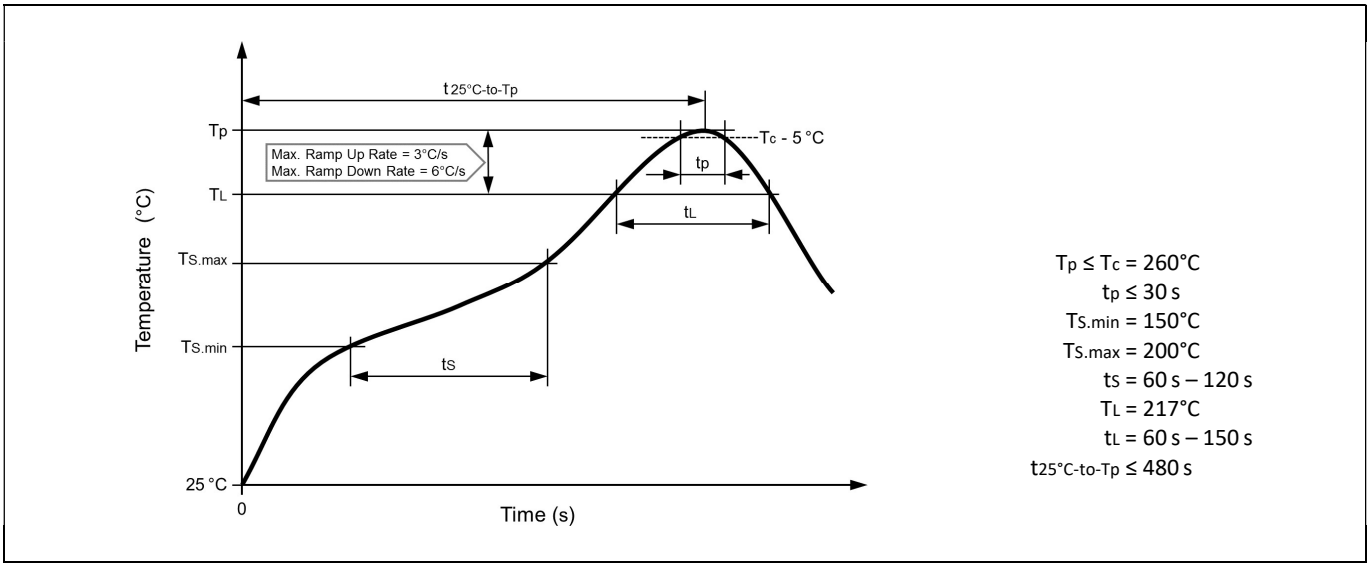


Figure 6 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

8 Measurement Results

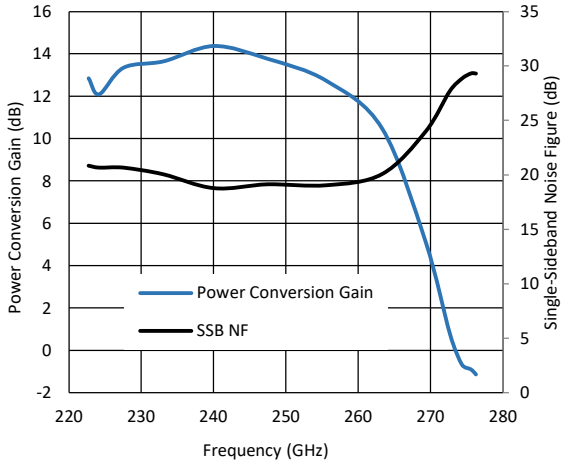


Figure 7 Power Conversion Gain and SSB Noise Figure for operation with internal VCO, measured at RX input (w/o antenna) for I-channel.

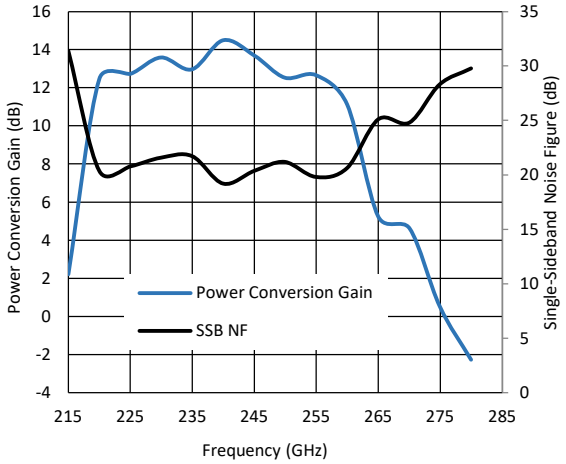


Figure 8 Power Conversion Gain and SSB Noise Figure for operation with external LO=0 dBm , measured at RX input (w/o antenna) for I-channel.

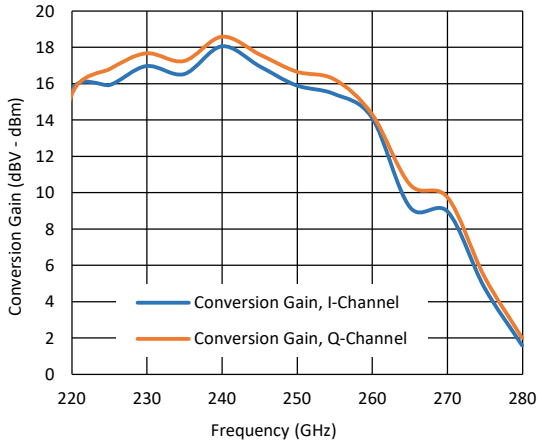


Figure 9 Conversion Gain for operation with internal VCO measured at antenna input.

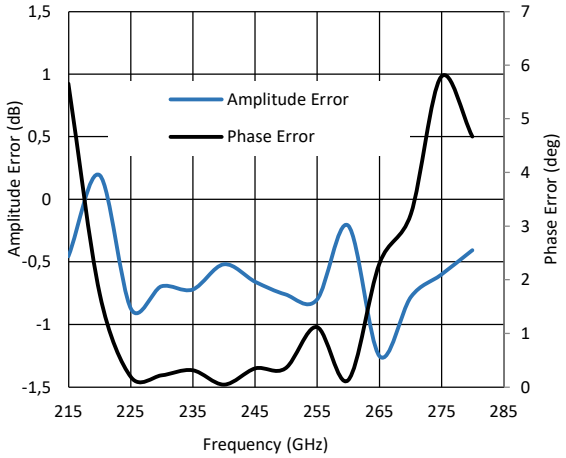


Figure 10 Measured Amplitude and Phase Error for operation with internal VCO.

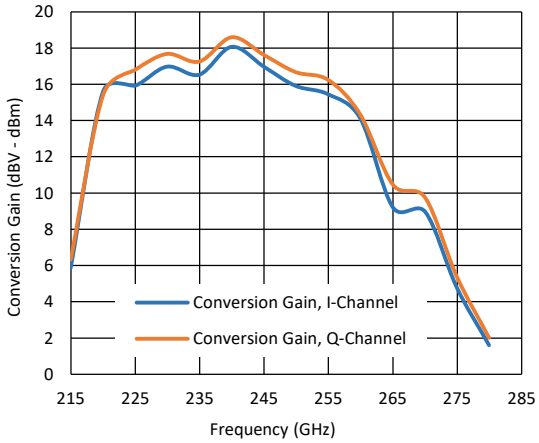


Figure 11 Conversion Gain for operation with external LO=0 dBm measured at antenna input measured at antenna input.

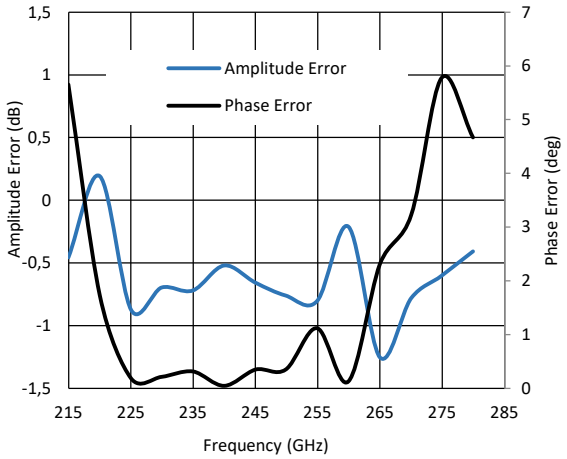


Figure 12 Measured Amplitude and Phase Error for operation with external LO=0 dBm.

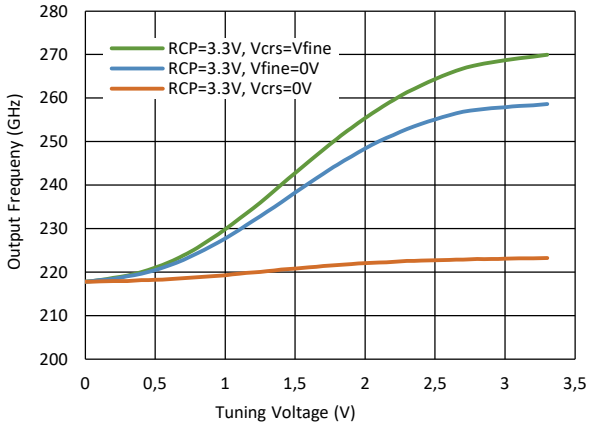


Figure 13 VCO Tuning Curves for RCP=3.3V.

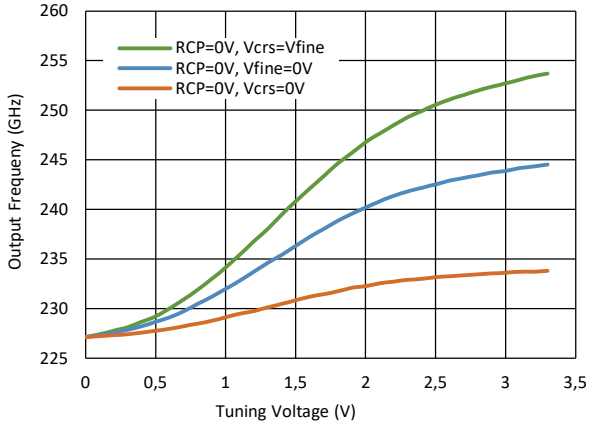


Figure 14 VCO Tuning Curves for RCP=0V.

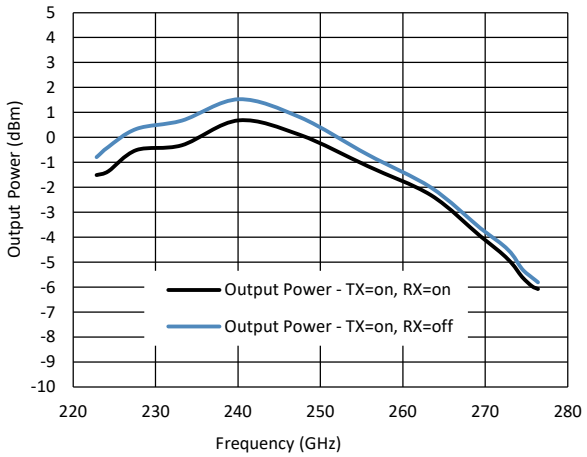


Figure 15 Output power measured at antenna input with internal VCO, TXEN=3.3V, TXpwr=0V.

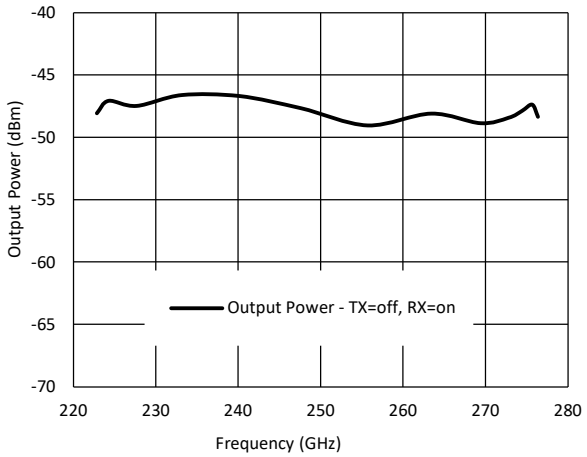


Figure 16 Output power measured at antenna input with internal VCO, TXEN=0V, TXpwr=0V.

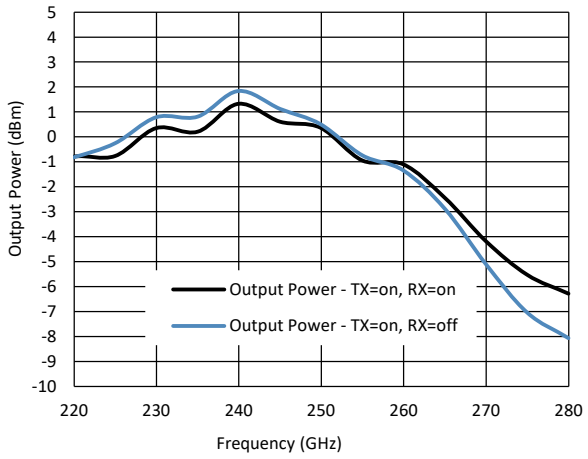


Figure 17 Output power measured at antenna input with external LO=0 dBm, TXEN=3.3V, TXpwr=0V.

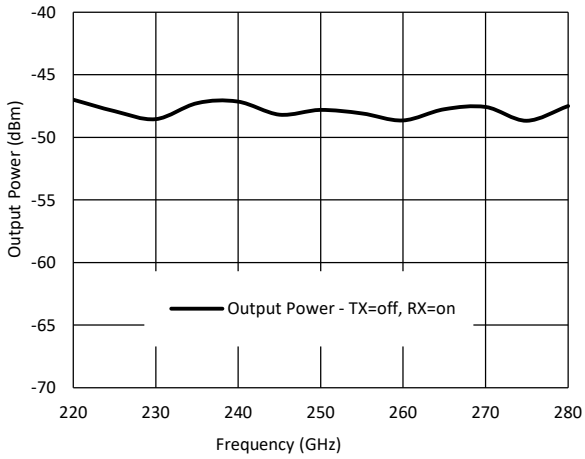


Figure 18 Output power measured at antenna input with external LO=0 dBm, TXEN=0V, TXpwr=0V.

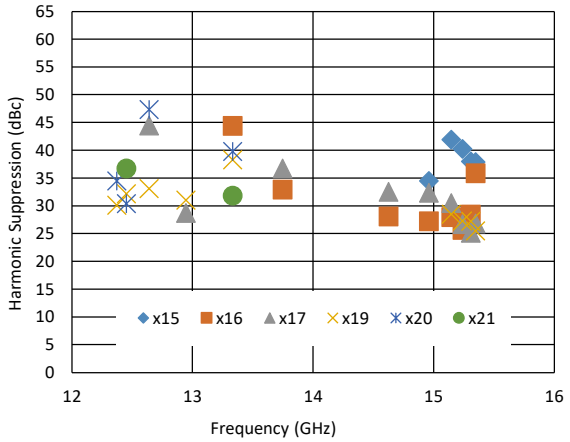


Figure 19 Harmonic suppression for operation with internal VCO.

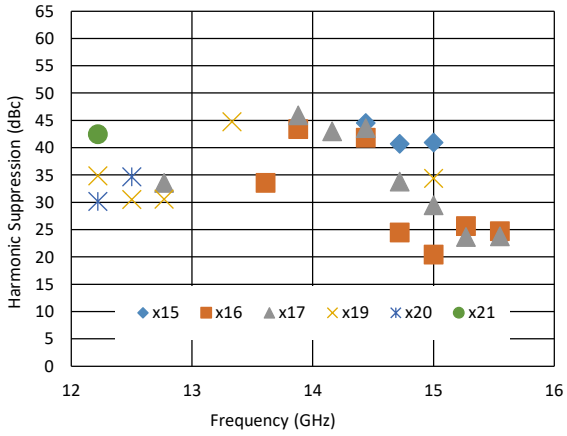


Figure 20 Harmonic suppression for operation with external LO=0 dBm.

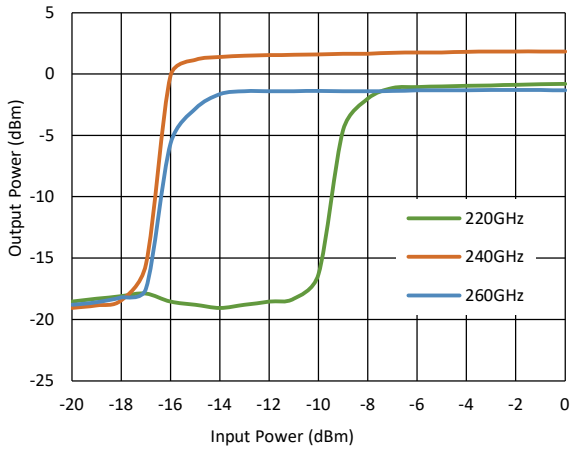


Figure 21 Output Power vs. LO input power.

The combined normalized radiation patterns of RX and TX antenna for FMCW operation are shown in following figures. During the measurement, the IC was operated in FMCW mode with a bandwidth of 1 GHz. A corner reflector was used as the target. The frequency of the measurement refers to the start frequency of the sweep.

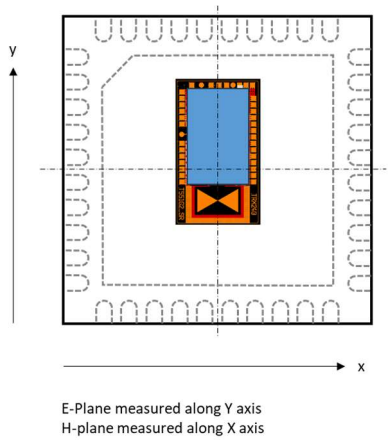


Figure 22 MMIC Orientation for Antenna Measurements. .

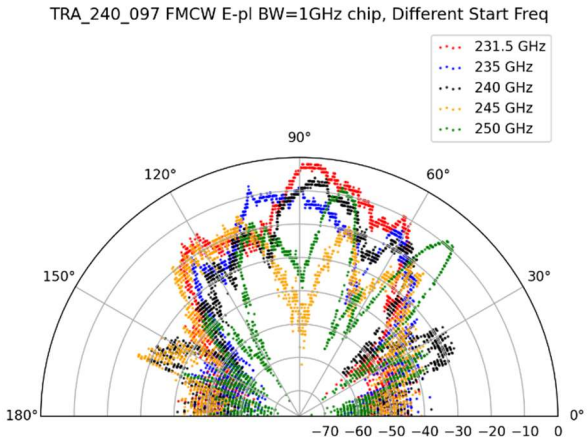


Figure 23 Combined Radiation Pattern of TX and RX Antennas – E-plane.

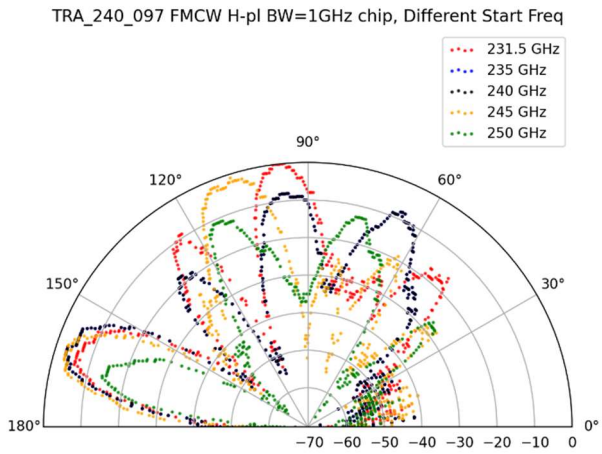


Figure 24 Combined Radiation Pattern of TX and RX Antennas – H-plane.

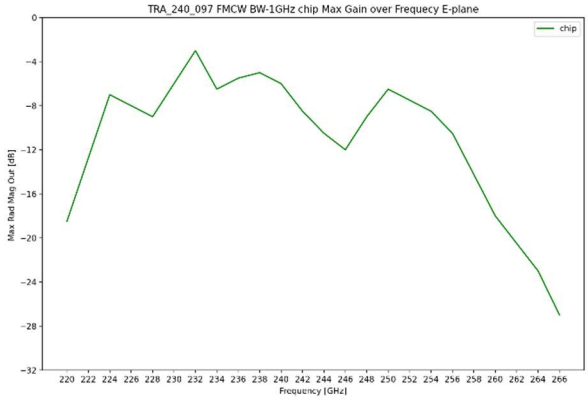


Figure 25 Measured Maximum Normalize Gain for Combined TX and RX Antennas – E-plane.

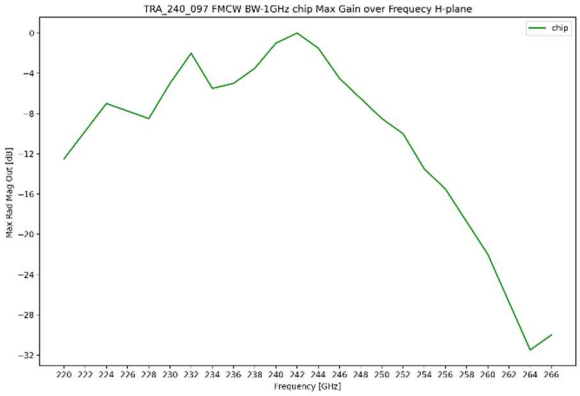


Figure 26 Measured Maximum Normalize Gain for Combined TX and RX Antennas – H-plane.

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